PRO-LOG®
CORPORATION

# STD 7000

# 7709
# 64K Memory Card

# USER'S MANUAL

A Pro-Log OPENWARE™ Product

5/85

## FOREWORD

This manual explains how to use the Pro-Log 7709 64K Memory Card. It is structured to reflect the answers to basic questions that you, the user, might ask yourself about the 7709. We welcome your suggestions on how we can improve our instructions.

The 7709 is an OPENWARE product in the Pro-Log Series 7000 STD BUS hardware. Our products are modular, and provide industrial managers with the means of using their own people to control the design, production, and maintenance of the products that use STD BUS hardware. Pro-Log also offers courses on how to design with and use microprocessors and the STD BUS products.

OPENWARE, a trademark of Pro-Log Corporation, means our products are designed to quality standards with readily available, second-sourced, industry standard components, clear and complete specifications, full documentation, and the option to purchase the manufacturing rights and drawings.

You may also find the following Pro-Log documents useful in your work: the **Microprocessor User's Guide** and the **STD BUS Technical Manual and Product Catalog**. If you would like a copy of these documents, please write to us on your company letterhead.

# Contents


| | Page |
|---|---|
| **Foreword** | ii |
| **Figures** | iv |
| **References/Bibliography** | v |
| **Section 1. Specifications** | 1-1 |
| Purpose | 1-1 |
| Features | 1-1 |
| Functional Description | 1-2 |
| Specifications | 1-3 |
| General | 1-3 |
| Electrical | 1-6 |
| Mechanical | 1-10 |
| **Section 2. Installation** | 2-1 |
| Introduction | 2-1 |
| Installation | 2-1 |
| Card Layout and Jumpers | 2-2 |
| Memory Bank Selection for the 16-Bit Address Bus | 2-4 |
| Bank Select Port Mapping (W1) | 2-4 |
| IOEXP (W2) | 2-5 |
| Memory Configuration | 2-5 |
| 20- or 16-Bit Address Bus (W8) | 2-5 |
| Memory Bank Size (W5) | 2-5 |
| Memory Mapping (W3) | 2-5 |
| Memory Mapping with the 20-Bit Address Bus | 2-5 |
| Memory Mapping with the 16-Bit Address Bus | 2-6 |
| MEMEX (W3) | 2-9 |
| Memory Socket Configuration (W4, W7, W9, W10) | 2-9 |
| Memory Socket Enable (W6) | 2-9 |
| Battery Source Selection (W12) | 2-9 |

| | Page |
|---|---|
| **Section 3. Operation and Programming** | 3-1 |
| Introduction | 3-1 |
| 20-Bit Address Bus | 3-1 |
| Memory Mapping | 3-2 |
| Memory Expansion with MEMEX | 3-3 |
| Memory Expansion with Multiple 7709 Cards | 3-3 |
| 16-Bit Address Bus | 3-3 |
| When to Use Bank Selection | 3-3 |
| No Bank Selection | 3-4 |
| 64K Bank Selection | 3-4 |
| 32K Bank Selection | 3-5 |
| Memory Expansion with MEMEX | 3-6 |
| Memory Expansion with Multiple 7709 Cards | 3-6 |
| Battery Backup | 3-7 |
| Data Retention Time | 3-7 |
| Powering UP and Down with Data Retention | 3-8 |
| Using VBATT for Battery Backup | 3-8 |
| Battery Low Indications | 3-8 |
| Write Inhibit Switches | 3-8 |
| **Section 4. Operating Software** | 4-1 |
| **Section 5. Maintenance** | 5-1 |
| Replacing the Battery | 5-1 |
| Reference Drawings | 5-1 |
| Return for Repair/Warranty | 5-8 |

# Figures


| Figure | | Page |
|---|---|---|
| 1-1 | 7709 64K Memory Card | 1-1 |
| 1-2 | Block Diagram | 1-2 |
| 1-3 | Configurations as Shipped | 1-3 |
| 1-4 | 20-Bit Memory Mapping Options | 1-4 |
| 1-5 | 16-Bit Memory Mapping Without Bank Selection or With 64K Bank Selection | 1-5 |
| 1-6 | 16-Bit Memory Mapping Options with 32K Bank Selection | 1-5 |
| 1-7 | Critical Memory Device Timing Parameters | 1-5 |
| 1-8 | Compatible Memory Devices | 1-5 |
| 1-9 | Memory Write Timing | 1-7 |
| 1-10 | Memory Read Timing | 1-8 |
| 1-11 | Bank Select Port Timing | 1-9 |
| 1-12 | P1 Connector Pinout | 1-10 |
| 1-13 | J1 Connector Pinout | 1-10 |
| 1-14 | J1 Compatible Connectors | 1-10 |
| 2-1 | Installation | 2-1 |
| 2-2 | Jumper Configuration | 2-2 |
| 2-3 | Sources for Shorting Connector | 2-2 |
| 2-4 | Physical Layout and Jumper Options | 2-2 |
| 2-5 | W1 Configured for Port EE Hex | 2-4 |
| 2-6 | Bank Select Port Mapping | 2-4 |
| 2-7 | W2 Configured for IOEXP Disabled | 2-5 |
| 2-8 | W8 Configured for a 20-Bit Address Bus | 2-5 |
| 2-9 | W5 Configured as a Contiguous 64K Bytes | 2-5 |
| 2-10 | W3 Configured for a Memory Starting Address of Hex 00000 | 2-5 |
| 2-11 | 20-Bit Memory Mapping | 2-6 |
| 2-12 | W3 Configured for No Bank Selection | 2-6 |
| 2-13 | W3 Configured for A Bank Address of Hex 06 | 2-6 |
| 2-14 | 64K Bank Address Jumper Configuration | 2-7 |
| 2-15 | W3 Configured for Bank Address 0A and 0B Hex | 2-8 |
| 2-16 | 32K Bank Address Jumper Configuration | 2-8 |
| 2-17 | W3 Configured for MEMEX Disabled | 2-9 |
| 2-18 | Memory Socket Configuration | 2-9 |
| 2-19 | W6 Configured to Enable all Eight Memory Sockets | 2-9 |
| 2-20 | W12 Configured for the 7709-XXN Nicad Battery | 2-9 |
| 3-1 | Configuring the 7709 for a 20-Bit Address Bus | 3-1 |
| 3-2 | 20-Bit Memory Mapping Options | 3-2 |
| 3-3 | 20-Bit Memory Mapping Example | 3-3 |
| 3-4 | 16-Bit Address Bus Options | 3-3 |
| 3-5 | Bank Selection | 3-4 |
| 3-6 | Configuring the 7709 for the 16-Bit Address Bus Without Bank Selection | 3-4 |
| 3-7 | Configuring the 7709 for the 16-Bit Address Bus With 64K Bank Selection | 3-5 |
| 3-8 | Bank Selecting 7709 Cards | 3-5 |
| 3-9 | Configuring the 7709 for the 16-Bit Address Bus With 32K Bank Selection | 3-5 |
| 3-10 | 32K Bank Selecting 7709 Cards | 3-6 |
| 3-11 | Using MEMEX and Bank Selection | 3-7 |
| 3-12 | Measuring Battery Standby Current | 3-7 |
| 3-13 | VBATT as a Source of Battery Backup | 3-8 |
| 3-14 | 7709-XXN Write Inhibit Switches | 3-8 |
| 5-1 | Schematic (7709-XXN with Battery Backup) | 5-2 |
| 5-2 | Schematic (7709-XX without Battery Backup) | 5-4 |
| 5-3 | Assembly Drawing (7709-XX with Battery Backup) | 5-6 |
| 5-4 | Assembly Drawing (7709-XX without Battery Backup) | 5-7 |

# REFERENCES/BIBLIOGRAPHY

**STD BUS Specification and Practice,** (Pro-Log Document #106989).

**Series 7000 STD BUS Technical Manual,** (Pro-Log Document #107855).

**Microprocessor User's Guide,** (Pro-Log Document #101145).

# Section 1
# SPECIFICATIONS

## PURPOSE

The 7709 is a versatile memory card that accepts up to 64K of 8Kx8-bit RAM or ROM devices. The 7709 operates in STD BUS systems using a 20-bit address bus (e.g., STD 8088) or in STD BUS systems using a 16-bit address bus (e.g., 8085 and Z80).

For systems using a 20-bit address bus, the 7709 demultiplexes the upper four address lines (A16-A19) from the lower four data lines (D0-D3) using the STD BUS MCSYNC* signal. In this mode of operation, the 7709 can be mapped into any 64K block of the one megabyte addressing space.

For systems using a 16-bit address bus, the 7709 provides a programmable bank select port to address more than 64K of memory in 32K or 64K banks.

Address decoding on the 7709 allows more than one card to be used in a system. In systems using a 20-bit address bus, multiple 7709s can provide the full one megabyte of directly addressable memory or two megabytes using the STD BUS MEMEX signal. In systems using a 16-bit address bus, multiple 7709s can be bank selected to provide four megabytes and up to eight megabytes using MEMEX.

## FEATURES

- Eight 28-pin JEDEC standard sockets
- Accepts 8Kx8-bit RAM or ROM
- 20-bit address bus decoding or 16-bit with optional bank selection (32K or 64K banks)
- Write inhibit switches
- Responds to MEMEX for memory expansion or bootstrapping
- Each socket can be jumper disabled to prevent wasted memory space
- Optional nicad battery backup for applications requiring nonvolatile RAM
- OPENWARE™ product
- Available in the following configurations:

| Model No. | Battery Backup | Populated RAM |
|---|---|---|
| 7709-00 | No | None |
| 7709-08 | No | 8K |
| 7709-16 | No | 16K |
| 7709-32 | No | 32K |
| 7709-64 | No | 64K |
| 7709-08N | Yes | 8K |
| 7709-16N | Yes | 16K |
| 7709-32N | Yes | 32K |
| 7709-64N | Yes | 64K |

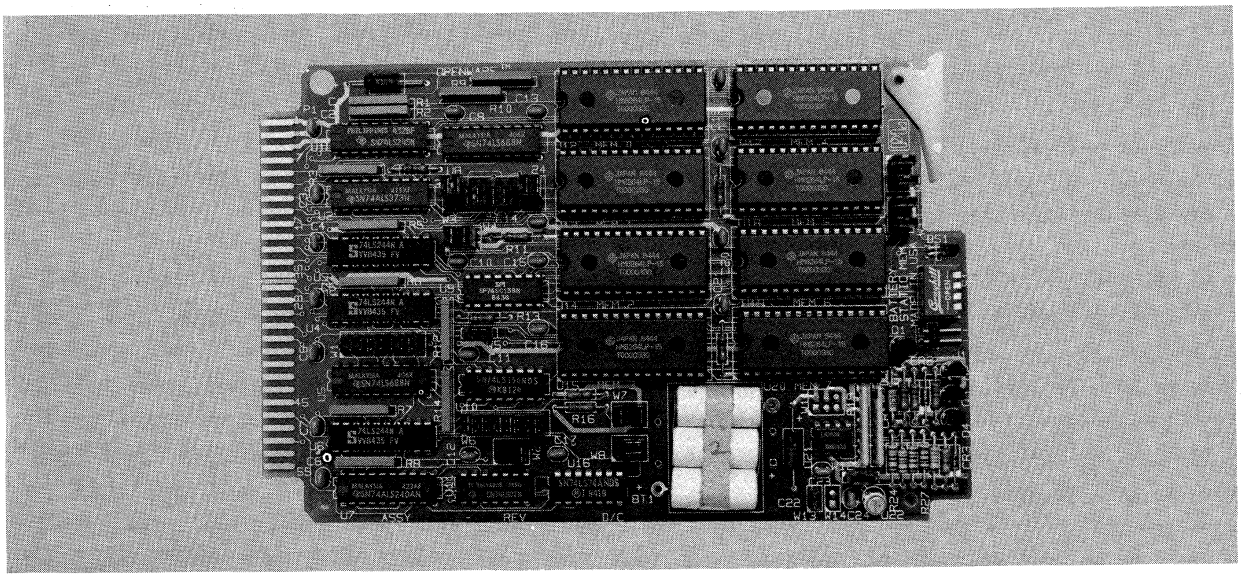


Figure 1-1. 7709 64K Memory Card

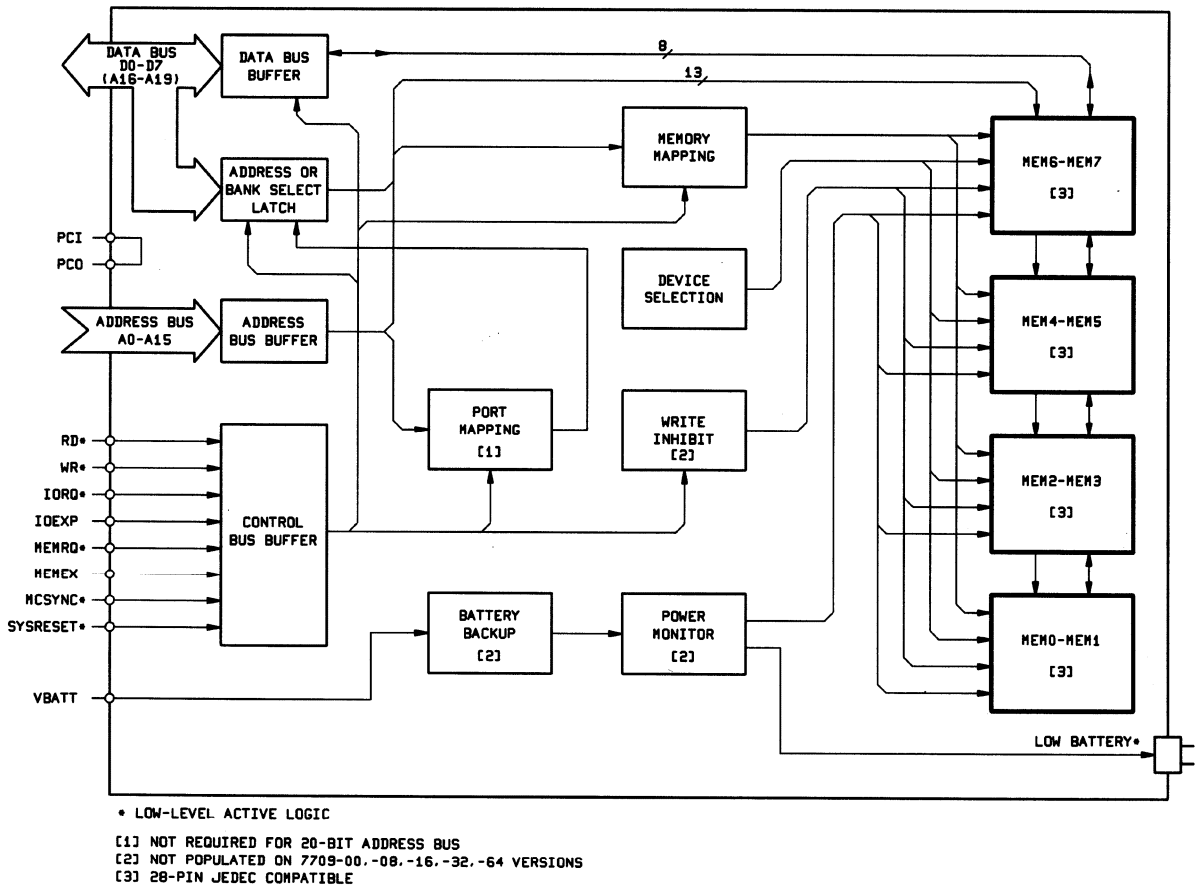



Figure 1-2. Block Diagram

## FUNCTIONAL DESCRIPTION

The functional description defines each block in the 7709 block diagram shown in figure 1-2. The block diagram and functional description are designed to familiarize the user with terms used throughout this manual.

**DATA BUS BUFFER.** The Data Bus Buffer provides buffering and direction control for the data bus signals D0-D7.

**ADDRESS OR BANK SELECT LATCH.** This latch serves a dual purpose. When the 7709 is operating in an STD BUS system using a 20-bit address bus (e.g., STD 8088), it demultiplexes the upper four-address lines (A16-A19) from the lower four data lines (D0-D3). When the 7709 is operating in an STD BUS system using a 16-bit address bus (e.g., STD 8085 and Z80), it is used as a programmable bank select port to permit large amounts of memory to be switched into use in 32K or 64K blocks.

**ADDRESS BUS BUFFER.** This buffer provides buffering for address bus signals A0-A15. For systems operating with a 20-bit address bus, the "Address or Bank Select Latch" is used to demultiplex the remaining four address lines, A16-A19. from the data bus.

**CONTROL BUS BUFFER.** The control signal interface between the STD BUS and the 7709 is provided by this buffer.

**PORT MAPPING.** This functional block selects the address of the port to be used for bank selection and is only required when the 7709 is operating with a 16-bit address bus and bank selection.

**MEMORY MAPPING.** Memory Mapping provides jumper selection of the address range for the memory on the 7709. The memory can be configured as a contiguous 64K bytes or two fully overlapped 32K bytes to be bank selected in software. In either configuration, each memory socket can be jumper disabled in 8K-byte blocks and used elsewhere in the STD BUS system. This prevents wasted memory space.

**DEVICE SELECTION.** Jumper selection of each socket pair is provided on the 7709 for one of the following configurations:

- 8Kx8-bit RAM
- 8Kx8-bit RAM without battery backup
- 8Kx8-bit RAM with battery backup

The 8Kx8 bit RAM with battery backup is only available on the 7709-XXN versions.

**MEMORY SOCKETS.** There are eight 28-pin JEDEC standard memory sockets on the 7709. They can be configured in pairs to accept 8Kx8-bit RAM or ROM.

**WRITE INHIBIT (on 7709-XX versions only).** The four write-inhibit switches prohibit the STD BUS WR* signal from reaching a RAM device. Each of the four write inhibit switches inhibits two RAM devices. A write-inhibited RAM device is functionally equivalent to ROM. Write inhibiting is useful in protecting debugged software during software development and power-up and power-down sequences.

**BATTERY BACKUP (on 7709-XXN vevsions only).** Data retention for battery-backed RAM devices is provided via a 3.6-volt nicad (rechargeable) battery when power is removed. Battery backup can also be provided by the STD BUS VBATT (pin 5) line.

**POWER MONITOR (for 7709-XXN versions only).** This monitor recharges the nicad battery when power is applied to the 7709. When power is removed from the 7709, the power monitor switches in the battery to provide standby current to battery-backed RAM devices. The power monitor is also responsible for protecting battery-backed RAM from spurious writes during power up and power down.

## SPECIFICATIONS

The 7709 operates in STD BUS systems with a 20-bit address bus (e.g., STD 8088) or a 16-bit address bus (e.g., STD 8085 and Z80). In some cases, the specifications depend upon which address bus is used. In these cases, the specifications are labeled 20-bit address bus or 16-bit address bus.

### General

**As Shipped:** The as-shipped configurations for the different versions of the 7709 are shown in figure 1-3.

| | | POPULATED MEMORY | |
|---|---|---|---|
| MODEL NUMBER | BATTERY BACKUP | AMOUNT (BYTES) | 20-BIT ADDRESS RANGE (HEX) |
| 7709-08N | Yes | 8K RAM | 00000-01FFF |
| 7709-16N | Yes | 16K RAM | 00000-03FFF |
| 7709-32N | Yes | 32K RAM | 00000-07FFF |
| 7709-64N | Yes | 64 RAM | 00000-0FFFF |
| 7709-00 | No | None | — |
| 7709-08 | No | 8K RAM | 00000-01FFF |
| 7709-16 | No | 16K RAM | 00000-03FFF |
| 7709-32 | No | 32K RAM | 00000-07FFF |
| 7709-64 | No | 64 RAM | 00000-0FFFF |

Figure 1-3. 7709 Configurations As Shipped

**Memory Mapping with the 20-Bit Address Bus:** The memory on the 7709 can be mapped anywhere within the address range provided by the 20-bit address bus. Figure 1-4 shows the address range of each memory socket for all 16 jumper-selectable options. Each socket can be independently disabled to tailor the 7709 to meet system requirements.

| | MEMORY SOCKET | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| OPTION | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| AS SHIPPED | 00000-01FFF | 02000-03FFF | 04000-05FFF | 06000-07FFF | 08000-09FFF | 0A000-0BFFF | 0C000-0DFFF | 0E000-0FFFF |
| 1 | 10000-11FFF | 12000-13FFF | 14000-15FFF | 16000-17FFF | 18000-19FFF | 1A000-1BFFF | 1C000-1DFFF | 1E000-1FFFF |
| 2 | 20000-21FFF | 22000-23FFF | 24000-25FFF | 26000-27FFF | 28000-29FFF | 2A000-2BFFF | 2C000-2DFFF | 2E000-2FFFF |
| 3 | 30000-31FFF | 32000-33FFF | 34000-35FFF | 36000-37FFF | 38000-39FFF | 3A000-3BFFF | 3C000-3DFFF | 3E000-3FFFF |
| 4 | 40000-41FFF | 42000-43FFF | 44000-45FFF | 46000-47FFF | 48000-49FFF | 4A000-4BFFF | 4C000-4DFFF | 4E000-4FFFF |
| 5 | 50000-51FFF | 52000-53FFF | 54000-55FFF | 56000-57FFF | 58000-59FFF | 5A000-5BFFF | 5C000-5DFFF | 5E000-5FFFF |
| 6 | 60000-61FFF | 62000-63FFF | 64000-65FFF | 66000-67FFF | 68000-69FFF | 6A000-6BFFF | 6C000-6DFFF | 6E000-6FFFF |
| 7 | 70000-71FFF | 72000-73FFF | 74000-75FFF | 76000-77FFF | 78000-79FFF | 7A000-7BFFF | 7C000-7DFFF | 7E000-7FFFF |
| 8 | 80000-81FFF | 82000-83FFF | 84000-85FFF | 86000-87FFF | 88000-89FFF | 8A000-8BFFF | 8C000-8DFFF | 8E000-8FFFF |
| 9 | 90000-91FFF | 92000-93FFF | 94000-95FFF | 96000-97FFF | 98000-99FFF | 9A000-9BFFF | 9C000-9DFFF | 9E000-9FFFF |
| 10 | A0000-A1FFF | A2000-A3FFF | A4000-A5FFF | A6000-A7FFF | A8000-A9FFF | AA000-ABFFF | AC000-ADFFF | AE000-AFFFF |
| 11 | B0000-B1FFF | B2000-B3FFF | B4000-B5FFF | B6000-B7FFF | B8000-B9FFF | BA000-BBFFF | BC000-BDFFF | BE000-BFFFF |
| 12 | C0000-C1FFF | C2000-C3FFF | C4000-C5FFF | C6000-C7FFF | C8000-C9FFF | CA000-CBFFF | CC000-CDFFF | CE000-CFFFF |
| 13 | D0000-D1FFF | D2000-D3FFF | D4000-D5FFF | D6000-D7FFF | D8000-D9FFF | DA000-DBFFF | DC000-DDFFF | DE000-DFFFF |
| 14 | E0000-E1FFF | E2000-E3FFF | E4000-E5FFF | E6000-E7FFF | E8000-E9FFF | EA000-EBFFF | EC000-EDFFF | EE000-EFFFF |
| 15 | F0000-F1FFF | F2000-F3FFF | F4000-F5FFF | F6000-F7FFF | F8000-F9FFF | FA000-FBFFF | FC000-FDFFF | FE000-FFFFF |

Figure 1-4. 20-Bit Memory Mapping Options

**Memory Mapping with the 16-Bit Address Bus:** The memory on the 7709 can be mapped anywhere within the address range provided by the 16-bit address bus. The 7709 operates in any one of three configurations: without bank selection, with 64K bank selection, or with 32K bank selection. Figure 1-5 shows the address range occupied by each memory socket when the 7709 is used without bank selection or with 64K bank selection. Figure 1-6 shows the address range occupied by each memory socket when the 7709 is used with 32K bank selection. In any configuration, each memory socket can be independently disabled to tailor the 7709 memory to meet system requirements.

| MEMORY SOCKET | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0000-1FFF | 2000-3FFF | 4000-5FFF | 6000-7FFF | 8000-9FFF | A000-BFFF | C000-DFFF | E000-FFFF |

Figure 1-5. 16-Bit Memory Mapping Without Bank Selection or With 64K Bank Selection

| | MEMORY SOCKET | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| OPTION | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 1 | 0000-1FFF | 2000-3FFF | 4000-5FFF | 6000-7FFF | 0000-1FFF | 2000-3FFF | 4000-5FFF | 6000-7FFF |
| 2 | 8000-9FFF | A000-BFFF | C000-DFFF | E000-FFFF | 8000-9FFF | A000-BFFF | C000-DFFF | E000-FFFF |

Figure 1-6. 16-Bit Memory Mapping Options with 32K Bank Selection

**Memory Devices:** The 7709 accepts 8Kx8-bit RAM or ROM. The memory devices must be compatible with the 28-pin JEDEC standard. Figure 1-7 shows the critical timing parameters for the memory devices and specific systems. The selected memory device must have values less than those shown. Refer to figures 1-9 and 1-10 for additional timing specifications.

The RAM devices selected for a battery-backed application must have standby currents of less than 50 microamps per device to meet the minimum data retention times shown in the Electrical Specifications.

Figure 1-8 lists memory devices that have been tested for use with the 7709.

| PARAMETER | DESCRIPTION | CRITICAL TIMES (NANOSECONDS) | | | | |
|---|---|---|---|---|---|---|
| | | STD 8085 | STDZ80 | | STD8088 | |
| | | 6.25 MHz | 2.5 MHz | 4.0 MHz | 5.0 MHz | 8.0 MHz |
| tOE | OE to output delay | 220 | 320 | 95 | 135 | 100 |
| tCE | CE to output delay | 415 | 450 | 200 | 325 | 180 |
| tWP | WR pulse width | 390 | 355 | 105 | 330 | 205 |
| tDW | Data setup time to WR | 400 | 540 | 385 | 270 | 150 |

Figure 1-7. Critical Memory Device Timing Parameters

| DEVICE | MANUFACTURER | PART NUMBER | |
|---|---|---|---|
| | | STD 8085, Z80 (2.5 MHz), 8088 (5.0 MHz) | STD Z80 (4.0 MHz) 8088 (8.0 MHz) |
| 8Kx8-BIT EPROM | Intel | 2764A-3 | 2764A-1 |
| | AMD | AM2764ADC-3 | — |
| 8Kx8-Bit RAM | Hitachi | HM6264LP-15 | HM6264LP-15 |
| | Toshiba | TC5564PL-15 | TC5564PL-15 |

Figure 1-8. Compatible Memory Devices

**Bank Select Port:** The bank select port is used to provide a software programmable bank selection. The bank select port address is jumper-programmable from 00 to FF hex. The bank select port address can be further qualified with the STD BUS IOEXP signal. The bank select port can be jumper-programmed to respond to IOEXP high, low, or not at all (disabled).

As shipped, the bank select port responds to output port address EE hex. IOEXP is disabled. If multiple 7709s are used in a system, the bank select port address should be the same for each.

## Electrical and Environmental

***Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise specified)***

- **Supply Voltage, Vcc 0 to 7 volts**
- **Operating Free-Air Temperature Range 0°C to 65°C**
- **Storage Temperature Range -40°C to +70°C**
- **Noncondensing Relative Humidity: 5% to 95%**

| Operating Conditions | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage, $V_{CC}$ | 4.75 | 5.00 | 5.25 | Volt |

| ELECTRICAL CHARACTERISTICS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless Otherwise Specified) | | | | |
|---|---|---|---|---|
| Parameter | MIN | TYP | MAX | UNIT |
| Supply Current, $I_{CC}$ | | | | |
| 7709-00 | — | 385 | 655 | mA |
| All others[1] | — | 440 | 775 | mA |
| Mean Time Between Failures, MTBF[2] | | | | |
| 7709-00 | — | 67 | — | * |
| 7709-08 | — | 60 | — | * |
| 7709-16 | — | 54 | — | * |
| 7709-32 | — | 46 | — | * |
| 7709-64 | — | 35 | — | * |
| 7709-08N | — | 36 | — | * |
| 7709-16N | — | 34 | — | * |
| 7709-32N | — | 30 | — | * |
| 7709-64N | — | 25 | — | * |

*Card Year/Failure

NOTES:

[1]The supply current of all populated versions is virtually the same. In all cases, only one device is selected at a time while the other devices are in standby mode and therefore consume a negligible (microamps) amount of current.

[2]MTBF calculations are based on component standard failure rates specified in "Failure Rates and MTBF," document #111443, revision C. The battery on the 7709-XXN version is not included.

Battery Type: Nicad

| Parameter | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Data Retention[3] | | | | |
| 7709-08N | 56 | 972 | — | Day |
| 7709-16N | 28 | 729 | — | Day |
| 7709-32N | 14 | 486 | — | Day |
| 7709-64N | 7 | 291 | — | Day |
| Battery Voltage | — | 3.6 | — | Volt |
| Battery Capacity[4] | — | 70 | — | mAH |
| Battery Charging Current | 4.5 | 7.0 | 25 | mA |
| Battery Charging Time[5] | — | — | 12 | Hour |
| Battery Switch-In Voltage | 4.48 | — | 4.75 | Volt |
| Battery Switch-Out Voltage | 4.36 | — | 4.62 | Volt |
| Hysteresis | — | 120 | — | mV |

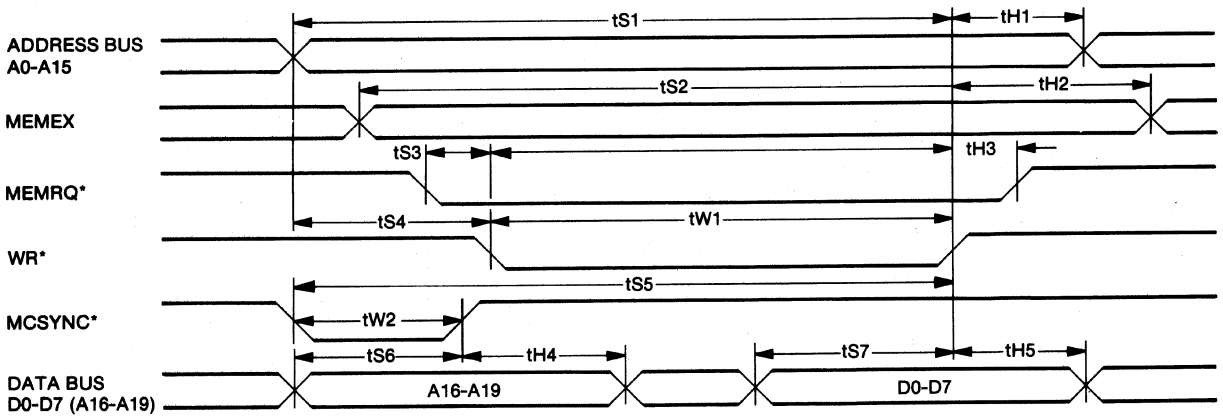
NOTES:

[3]For a fully charged battery with memory devices having a standby current of 20 μa typical and 50 μa maximum. (Note that maximum standby current results in minimum data retention.)

[4]Battery capacity from a fully charged battery, discharged at 20°C for 5 hours to a 3-volt cutoff.

[5]For a fully discharged battery at 25°C.

All logic signal levels related to the 7709 that appear on the STD BUS conform to the STD BUS TTL requirements as specified in the general *STD Series 7000 Specification,* document #111684, revision B.




| PARAMETER | DESCRIPTION | NANOSECONDS 1 MIN | NANOSECONDS 1 MAX | NANOSECONDS 2 MIN | NANOSECONDS 2 MAX |
|---|---|---|---|---|---|
| tH1 | A0-A15 hold from WR* inactive | 27 | | 17+tWR | |
| tH2 | MEMEX hold from WR* inactive | 19 | | 9+tWR | |
| tH3 | MEMRQ* hold from WR* inactive | 0 | | 0+tDH | |
| tH4 | A16-A19 hold from MCSYNC* inactive | 18 | | 18[4] | |
| tH5 | D0-D7 hold from WR* inactive | 19 | | 19+tDH | |
| tS1 | A0-A15 setup to WR* inactive | 228 | | 108+tCW<br>17+tAW[3] | |
| tS2 | MEMEX setup to WR* inactive | 217 | | 97+tCW | |
| tS3 | MEMRQ* setup to WR* inactive | 77 | | 77 | |
| tS4 | A0-A15 setup to WR* inactive | 27 | | 17+tAS | |
| tS5 | MCSYNC* setup to WR* inactive | 246 | | 125+tCW[4] | |
| tS6 | A16-A19 setup to MCSYNC* inactive | 8 | | 8[4] | |
| tS7 | D0-D7 setup to WR* inactive | 70 | | 10+tDW | |
| tW1 | WR* pulse width | 95 | | 5+tWP | |
| tW2 | MCSYNC* pulse width | 15 | | 15[4] | |

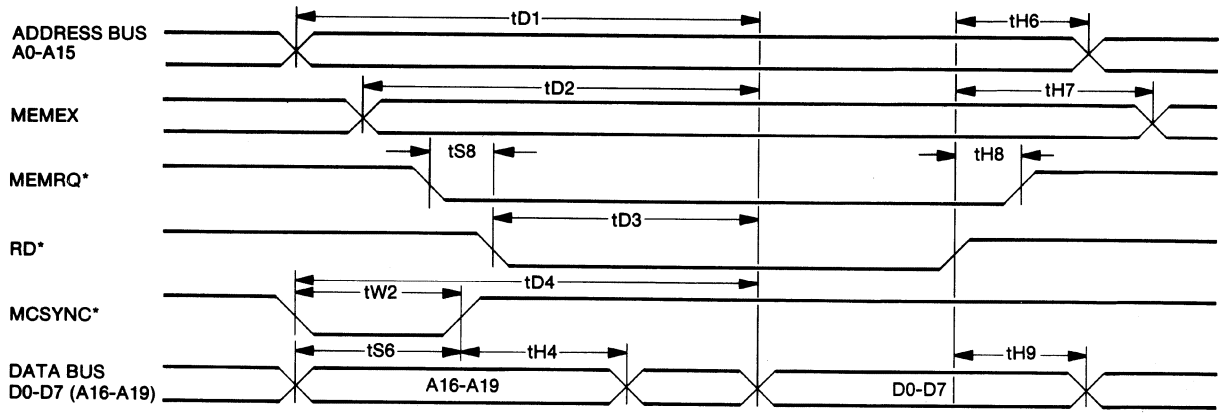
[1]Populated versions

[2]Unpopulated versions:
tAW=Address valid to WR inactive
tWR=CSI hold from WR inactive
tDH=Data hold from WR inactive
tCW=CSI setup to WR inactive
tAS=Address setup to WR active
tDW=Data setup to WR inactive
tWP=Write pulse width

[3]Whichever is longest

[4]For 20-bit address bus only.

Figure 1-9. Memory Write Timing




| PARAMETER | DESCRIPTION | NANOSECONDS | | | |
|---|---|---|---|---|---|
| | | 1 | | 2 | |
| | | MIN | MAX | MIN | MAX |
| tD1 | Delay from A0-A15 to D0-D7 | | 246 | | 96+tCE[3]<br>39+tACC |
| tD2 | Delay from MEMEX to D0-D7 | | 262 | | 112+tCE |
| tD3 | Delay from RD* to D0-D7 | | 109 | | 39+tOE |
| tD4 | Delay from MCSYNC* to D0-D7 | | 280 | | 130+tCE[4] |
| tH4 | A16-A19 hold from MCSYNC* inactive | 18 | | 18[4] | |
| tH6 | A0-A15 hold from RD* inactive | 0 | | 0 | |
| tH7 | MEMEX hold fromRD* inactive | 0 | | 0 | |
| tH8 | MEMRQ* hold from RD* inactive | 0 | | 0 | |
| tH9 | D0-D7 hold from RD* inactive | 13 | | 13 | |
| tS6 | A16-A19 setup to MCSYNC* inactive | 8 | | 8[4] | |
| tS8 | MEMRQ* setup to RD* inactive | 77 | | 77 | |
| tW2 | MCSYNC* pulse width | 15 | | 15[4] | |

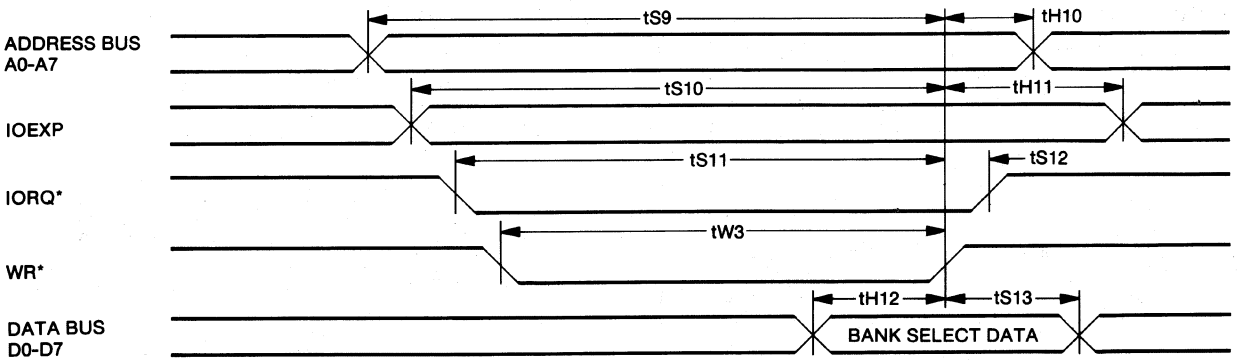
[1]Populated versions.

[2]Unpopulated versions:
tCE=CE to output delay
tACC=Address to output delay
tOE=OE to output delay
tOH=Output hold from OE

[3]Whichever is longest.

[4]For the 20-bit address bus only.

Figure 1-10. Memory Read Timing




| | | NANOSECONDS | |
|---|---|---|---|
| PARAMETER | DESCRIPTION | MIN | MAX |
| tH10 | A0-A7 hold after WR* inactive | 18 | |
| tH11 | IOEXP hold after WR* inactive | 60 | |
| tH12 | IORQ* hold after WR* inactive | 71 | |
| tH13 | D0-D7 hold ater WR* inactive | 48 | |
| tS9 | A0-A7 setup to WR* inactive | 38 | |
| tS10 | IOEXP setup to WR* inactive | 60 | |
| tS11 | IORQ* setup to WR* inactive | 57 | |
| tS12 | D0-D7 setup to WR* active | 0 | |
| tW3 | WR* pulse width | 20 | |

Figure 1-11. Bank Select Port Timing

## Mechanical

The 7709 meets all general mechanical specifications of the STD BUS Series 7000 as given in the general STD Series 7000 Specification, document #111684, revision B, except that the 7709-XXN versions require one 0.625-inch (15.875 mm) card slot.

| PIN NUMBER | | | | PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|
| OUTPUT (LSTTL DRIVE) | | | | | | OUTPUT (LSTTL DRIVE) | |
| INPUT (LSTTL LOADS) | | | | | | | INPUT (LSTTL LOADS) |
| MNEMONIC | | | | | | | MNEMONIC |
| +5V | IN | | 2 | 1 | | IN | +5V |
| GROUND | IN | | 4 | 3 | | IN | GROUND |
| DCPWRDWN* | | | 6 | 5 | | IN | VBATT |
| D7 | 1 | 55 | 8 | 7 | 55 | 1 | D3 |
| D6 | 1 | 55 | 10 | 9 | 55 | 1 | D2 |
| D5 | 1 | 55 | 12 | 11 | 55 | 1 | D1 |
| D4 | 1 | 55 | 14 | 13 | 55 | 1 | D0 |
| A15 | 1 | | 16 | 15 | | 1 | A7 |
| A14 | 1 | | 18 | 17 | | 1 | A6 |
| A13 | 1 | | 20 | 19 | | 1 | A5 |
| A12 | 1 | | 22 | 21 | | 1 | A4 |
| A11 | 1 | | 24 | 23 | | 1 | A3 |
| A10 | 1 | | 26 | 25 | | 1 | A2 |
| A9 | 1 | | 28 | 27 | | 1 | A1 |
| A8 | 1 | | 30 | 29 | | 1 | A0 |
| RD* | 1 | | 32 | 31 | | 1 | WR* |
| MEMRQ* | 1 | | 34 | 33 | | 1 | IORQ* |
| MEMEX | 1 | | 36 | 35 | | 1 | IOEXP |
| MCSYNC* | 1 | | 38 | 37 | | | REFRESH* |
| STATUS 0* | | | 40 | 39 | | | STATUS 1* |
| BUSRQ* | | | 42 | 41 | | | BUSAK* |
| INTRQ* | | | 44 | 43 | | | INTAK* |
| NMIRQ* | | | 46 | 45 | | | WAITRQ* |
| PBRESET* | | | 48 | 47 | | 1 | SYSRESET* |
| CNTRL* | | | 50 | 49 | | | CLOCK* |
| PCI | IN | | 52 | 51 | OUT | | PCO |
| AUX GND | | | 54 | 53 | | | AUX GND |
| AUX -V | | | 56 | 55 | | | AUX +V |

* Low-level active logic
1 LSTTL Load = -0.4 mA

Figure 1-12. P1 Connector Pinout

## 7709 User Interface

The 7709 has onboard circuitry to monitor the battery voltage. When the battery voltage drops below approximately 2.4 volts, the Battery Low LED illuminates and a normally active-high signal at J1 goes low.

| PIN NUMBER | | | | PIN NUMBER | | | |
|---|---|---|---|---|---|---|---|
| OUTPUT (LSTTL DRIVE) | | | | | | OUTPUT (LSTTL DRIVE) | |
| INPUT (LSTTL LOADS) | | | | | | | INPUT (LSTTL LOADS) |
| MNEMONIC | | | | | | | MNEMONIC |
| GROUND | IN | | 1 | 2 | 35 | | LOW BATTERY* |

Figure 1-13. J1 Connector Pinout

Twisted pair cable assemblies are available from Pro-Log: The RC704-1 is a 12-inch cable and the RC704-2 is a 16-inch cable. Compatible mating connectors are shown in Figure 1-14.

| MANUFACTURER | HOUSING | SOCKET |
|---|---|---|
| AMP | 530554-1 | 530553-5 |
| BERG | 65039-035 | 75691-015 |

NOTE: Housings and sockets cannot be mixed between manufacturers. Also note that this list is for customer convenience. Many other manufacturers' connectors are compatible. For more information, consult manufacturers' catalogs.

Figure 1-14. J1 Compatible Connectors

# Section 2
# INSTALLATION

## INTRODUCTION

This section describes the procedure for installing the 7709 card into an STD BUS system. Options and specifications are included that must be considered before this card is installed. This section does not explain the operation of the 7709 as it is reviewed in section 3.

## INSTALLATION

**CAUTION**

To prevent possible damage to your STD BUS system, make sure power is **off** before inserting a card into the card rack or before removing a card from the card rack.

The 7709 is designed to operate as part of an STD BUS system. The 7709 can be inserted into any slot in the STD BUS card rack with the ejector tab at the top as illustrated in figure 2-1. If access to the card is needed for testing or servicing, a card extender such as the Pro-Log 7901 may be used.

**BATTERY BACKUP**

The nicad battery on 7709-XXN versions must be recharged before providing data retention. The 7709-XXN must remain under power for a minimum of 12 hours to fully charge a discharged battery.

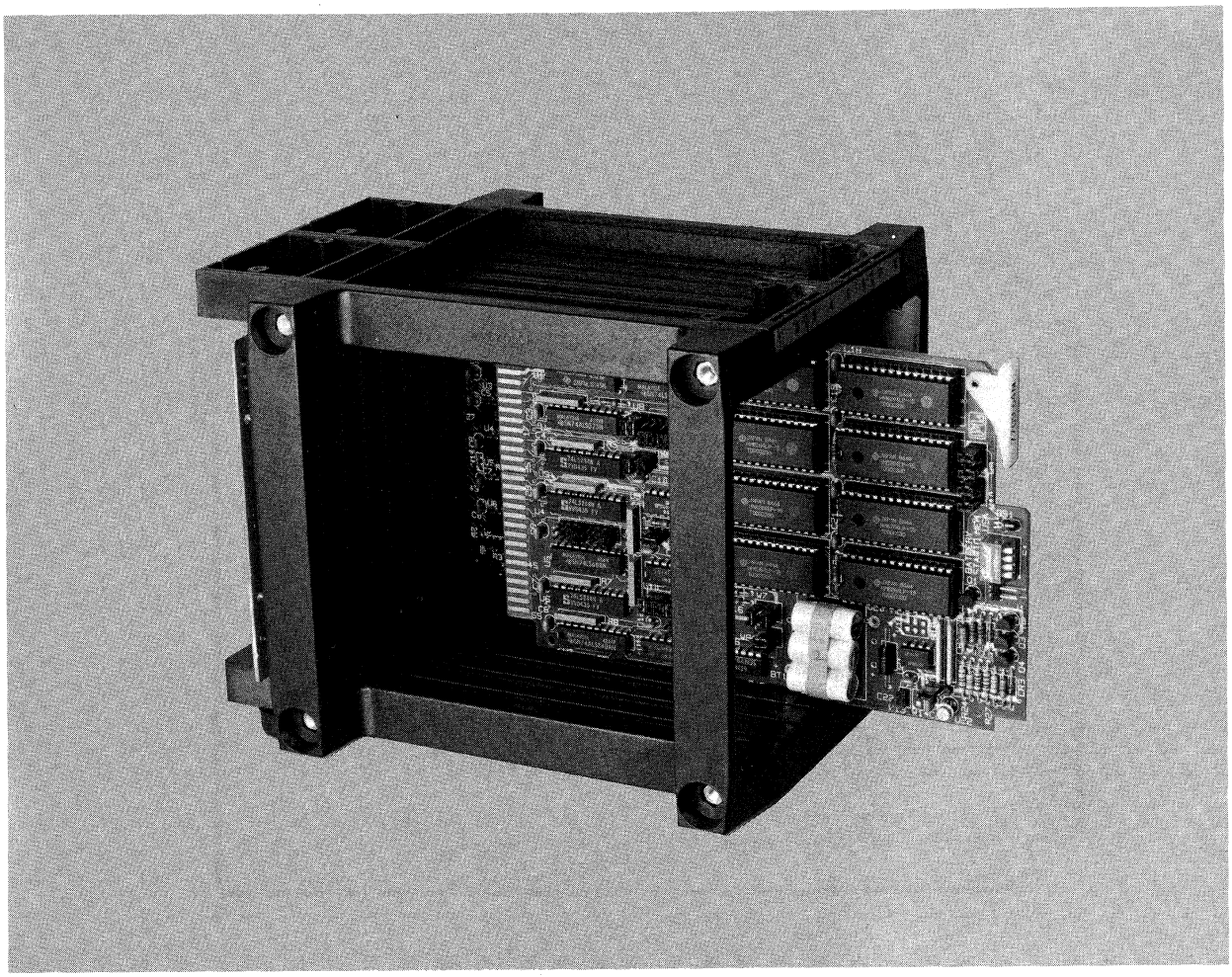


Figure 2-1. Installation

## CARD LAYOUT AND JUMPERS

The 7709 has onboard jumpers to configure the card to meet system requirements. The jumper configurations consist of unshrouded headers and shorting connectors, as shown in figure 2-2. The shorting connectors can be removed and installed without the use of soldering equipment. Figure 2-3 lists sources for the shorting connectors.

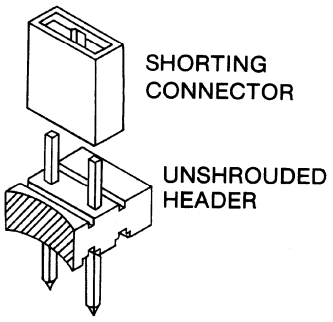



Figure 2-2. Jumper Configuration

| MANUFACTURER | HOUSING | SOCKET |
|---|---|---|
| AMP | 530554-1 | 530553-5 |
| BERG | 65039-035 | 75691-015 |

Figure 2-3. Sources for Shorting Connector

Figure 2-4 provides a reference for the location and a brief description of each jumper on the 7709. The explanations of the jumpers are divided into three functional groups: Memory Bank Selection with the 16-Bit Address Bus, Memory Configuration, and Battery Backup. Refer to section 3 for information on jumper options required for specific applications.

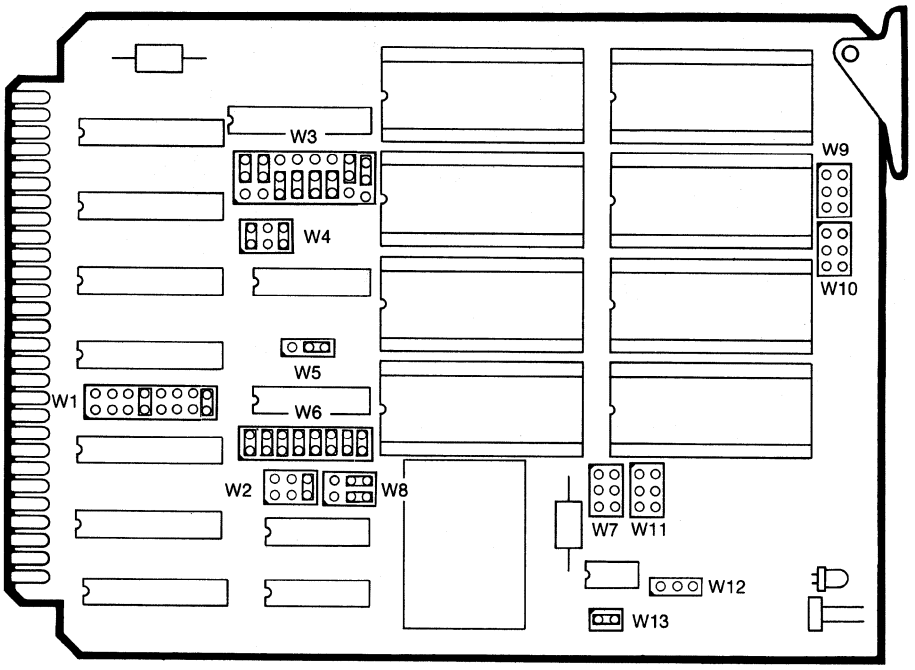



Figure 2-4. Physical Layout and Jumper Options

| JUMPER GROUP | JUMPER INSTALLED | JUMPER REMOVED | DESCRIPTION | AS SHIPPED | SEE PAGE |
|---|---|---|---|---|---|
| W1 | — | — | BANK SELECT PORT MAPPING<br>• See figure 2-6 | | 2-4 |
| W2 | | | IOEXP | | 2-5 |
| | 1-2 | 3-4, 5-6 | • Active low | | |
| | 3-4 | 1-2, 5-6 | • Active high | | |
| | 5-6 | 1-2, 3-4 | • Disabled | * | |
| W3 | | | MEMORY MAPPING | | 2-5 |
| | | | • 20-Bit Address Bus (see figure 2-11) | * | |
| | | | • 16-Bit Address Bus<br>—No bank selection (see fig. 2-12)<br>—64K bank selection (see fig. 2-14)<br>—32K bank selection (see fig. 2-16) | | |
| | | | MEMEX | | 2-9 |
| | 22-23 | | • Active low | | |
| | | 22-23, 23-24 | • Active high | | |
| | 23-24 | | • Disabled | | |
| W4 | | | MEM 0, 1 SOCKET CONFIGURATION | (1) | 2-9 |
| | 3-4 | 1-2, 5-6 | • 8K ROM | | |
| | 1-2, 3-4 | 5-6 | • 8K RAM without battery backup | | |
| | 1-2, 5-6 | 3-4 | • 8K RAM with battery backup | | |
| W5 | | | MEMORY BANK SIZE | | 2-5 |
| | 2-3 | | • 64K or no bank selection | * | |
| | 1-2 | | • 32K bank selection | | |
| W6 | | | MEMORY SOCKET ENABLE | | 2-9 |
| | 1-2 | | • Enable socket 7 | * | |
| | 3-4 | | • Enable socket 6 | * | |
| | 5-6 | | • Enable socket 5 | * | |
| | 7-8 | | • Enable socket 4 | * | |
| | 9-10 | | • Enable socket 3 | * | |
| | 11-12 | | • Enable socket 2 | * | |
| | 13-14 | | • Enable socket 1 | * | |
| | 15-16 | | • Enable socket 0 | * | |
| W7 | | | MEM 2, 3 SOCKET CONFIGURATION | (1) | 2-9 |
| | 3-4 | 1-2, 5-6 | • 8K ROM | | |
| | 1-2, 3-4 | 5-6 | • 8K RAM without battery backup | | |
| | 1-2, 5-6 | 3-4 | • 8K RAM with battery backup | | |
| W8 | | | 20- or 16-BIT ADDRESS BUS | | 2-5 |
| | 3-5, 4-6 | | • 20-bit address bus | * | |
| | 1-2, 5-6 | | • 16-bit address bus | | |
| W9 | | | MEM 4, 5 SOCKET CONFIGURATION | (1) | 2-9 |
| | 3-4 | 1-2, 5-6 | • 8K ROM | | |
| | 1-2, 3-4 | 5-6 | • 8K RAM without battery backup | | |
| | 1-2, 5-6 | 3-4 | • 8K RAM with battery backup | | |
| W10 | | | MEM 6, 7 SOCKET CONFIGURATION | (1) | 2-9 |
| | 3-4 | 1-2, 5-6 | • 8K ROM | | |
| | 1-2, 3-4 | 5-6 | • 8K RAM without battery backup | | |
| | 1-2, 5-6 | 3-4 | • 8K RAM with battery backup | | |
| W11 | | | FOR PRO-LOG USE ONLY | | |
| W12 | | | BATTERY BACKUP SOURCE (-XXN versions) | | 2-9 |
| | 1-2 | 3-4 | • On card battery | * | |
| | 3-4 | 1-2 | • STD BUS VBATT | | |
| W13 | | | FOR PRO-LOG USE ONLY | | |

(1) The as-shipped configuration is version dependent.

Figure 2-4 (Continued)

## Memory Bank Selection for a 16-Bit Address Bus

Jumper groups W1 and W2 only affect a 7709 configured for bank selection. Bank selection is a technique used when an STD BUS system requires more memory than can be directly addressed by the CPU. In a system with a 16-bit address bus, bank selection can be used when more than 64K of combined RAM and ROM is required. Bank selection is discussed in detail in section 3.

**Bank Select Port Mapping (W1):** The 7709 decodes one output port to be used for software programmable bank selection. Using W1, the bank select port address can be jumper selected anywhere in the range from hex 00 to FF. Figure 2-5 shows W1 configured for port EE. This is the as-shipped configuration for the 7709.

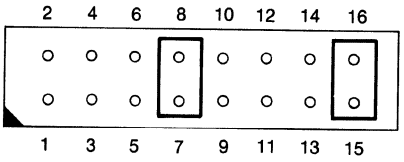



Figure 2-5. W1 Configured for Port EE Hex

Figure 2-6 provides the jumper information necessary to configure the bank select port address. For example, assume that the bank select port is to be mapped at hex C8. According to figure 2-6, this would require W1 jumpers to be placed at the following positions only: 5-6, 7-8, 11-12, 13-14, and 15-16.

| W1 JUMPER POSITION | | | | UPPER | |
|---|---|---|---|---|---|
| 1-2 (A7) | 3-4 (A6) | 5-6 (A5) | 7-8 (A4) | HEX DIGIT | AS SHIPPED |
| X | X | X | X | 0 | |
| X | X | X | | 1 | |
| X | X | | X | 2 | |
| X | X | | | 3 | |
| X | | X | X | 4 | |
| X | | X | | 5 | |
| X | | | X | 6 | |
| X | | | | 7 | |
| | X | X | X | 8 | |
| | X | X | | 9 | |
| | X | | X | A | |
| | X | | | B | |
| | | X | X | C | |
| | | X | | D | |
| | | | X | E | * |
| | | | | F | |

| W1 JUMPER POSITION | | | | LOWER | |
|---|---|---|---|---|---|
| 9-13 (A3) | 11-12 (A2) | 13-14 (A1) | 15-16 (A0) | HEX DIGIT | AS SHIPPED |
| X | X | X | X | 0 | |
| X | X | X | | 1 | |
| X | X | | X | 2 | |
| X | X | | | 3 | |
| X | | X | X | 4 | |
| X | | X | | 5 | |
| X | | | X | 6 | |
| X | | | | 7 | |
| | X | X | X | 8 | |
| | X | X | | 9 | |
| | X | | X | A | |
| | X | | | B | |
| | | X | X | C | |
| | | X | | D | |
| | | | X | E | * |
| | | | | F | |

X = Jumper installed
*As shipped, the 7709 bank select port is at hex EE

Figure 2-6. Bank Select Port Mapping

**IOEXP (W2):** IOEXP is an STD BUS signal that can be used to expand the number of I/O ports in an STD BUS system. Using W2, the 7709 can be configured to respond to IOEXP high, IOEXP low, or not to respond to IOEXP at all (disabled). Figure 2-7 shows W2 configured for IOEXP disabled. This is the as-shipped configuration for the 7709.

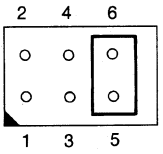



Figure 2-7. W2 Configured for IOEXP Disabled

To enable IOEXP, refer to figure 2-4, page 2-3 for correct jumper position. For example, assume that the bank select port is to be enabled only when IOEXP is in the high state. According to figure 2-4, this would require W2 jumpers to be installed in position 3-4 only.

## Memory Configuration

The 7709 is a versatile memory card that operates in STD BUS systems with either a 20- or 16-bit address bus. In addition, the memory on the 7709 can be mapped anywhere in the memory range of either STD BUS system. The following explains the jumpers used to configure the 7709 memory to meet individual system requirements.

**20- or 16-Bit Address Bus (W8):** The 7709 operates in STD BUS systems using a 20-bit address bus (e.g., STD 8088) or in STD BUS systems using a 16-bit address bus (e.g., STD 8085 and Z80). W8 is used to configure the 7709 for either the 20-bit or the 16-bit address bus. Figure 2-8 shows W8 configured for a 20-bit address bus. This is the as-shipped configuration for the 7709.

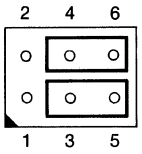



Figure 2-8. W8 Configured for a 20-Bit Address Bus

Figure 2-4, page 2-3, provides the jumper information necessary to configure W8. For example, assume that the 7709 is to operate with a 16-bit address bus. According to figure 2-4, this would require a jumper at positions 1-3 and 2-4 of W8.

**Memory Bank Size (W5):** The memory bank size must be jumper configured whether or not bank selection is used. The 7709 memory can be configured as one contiguous 64K bank or as two fully overlapped 32K banks to be bank selected. Figure 2-9 shows W5 configured for a 64K contiguous bank of memory. This is the as-shipped configuration on the 7709.

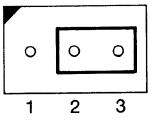



Figure 2-9. W5 Configured as a Contiguous 64K Bytes

Figure 2-4, page 2-3, provides the jumper information necessary to configure W5. For example, assume that the memory on the 7709 is to be bank selected in banks of 32K bytes. According to figure 2-4, this would require a jumper at position 1-2 of W5.

**Memory Mapping (W3):** W3 is used to map the memory on the 7709 into the CPU addressing space and to select the 7709 response to MEMEX. The function of W3 differs for 20-bit address bus and 16-bit address bus operations. The following discussion of memory mapping is divided into two categories: 20-bit address bus and 16-bit address bus. The MEMEX jumper group functions the same for either configuration.

**Memory Mapping with the 20-Bit Address Bus:** The 7709 supports eight contiguously mapped memory sockets (MEM 0 through MEM 7), each capable of supporting an 8Kx8-bit memory device. W3 is used to select the starting address of the contiguous block of memory. The address range depends upon the number of populated memory sockets. Figure 2-10 shows W3 configured for a starting address of hex 00000. This is the as-shipped configuration for the 7709.

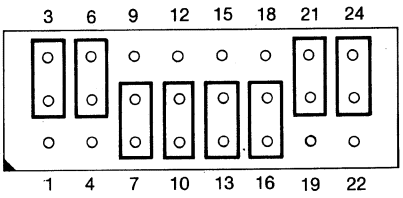



Figure 2-10. W3 Configured for a Memory Starting Address of Hex 00000

It is important to note that only the center four jumper positions are used in memory mapping the 7709 for a 20-bit address bus. The jumpers at positions 2-3, 5-6, and 20-21 must remain as shown in figure 2-10. The right-most jumper is used for MEMEX and may or may not be in the position shown.

Figure 2-11 provides the jumper information necessary to configure W3 for 20-bit memory mapping. For example, assume that memory is required to start at hex 50000. According to figure 2-11, this would require jumpers to be placed in the following positions only: 2-3, 5-6, 7-8, 13-14, and 20-21.

| W3 JUMPER POSITION | | | | | | | 20-BIT | AS |
|---|---|---|---|---|---|---|---|---|
| 2-3 | 5-6 | 7-8 (A19) | 10-11 (A18) | 13-14 (A17) | 16-17 (A16) | 20-21 | ADDRESS RANGE | SHIP-PED |
| X | X | X | X | X | X | X | 00000-0FFFF | * |
| X | X | X | X | X | | X | 10000-1FFFF | |
| X | X | X | X | | X | X | 20000-2FFFF | |
| X | X | X | X | | | X | 30000-3FFFF | |
| X | X | X | | X | X | X | 40000-4FFFF | |
| X | X | X | | X | | X | 50000-5FFFF | |
| X | X | X | | | X | X | 60000-6FFFF | |
| X | X | X | | | | X | 70000-7FFFF | |
| X | X | | X | X | X | X | 80000-8FFFF | |
| X | X | | X | X | | X | 90000-9FFFF | |
| X | X | | X | | X | X | A0000-AFFFF | |
| X | X | | X | | | X | B0000-BFFFF | |
| X | X | | | X | X | X | C0000-CFFFF | |
| X | X | | | X | | X | D0000-DFFFF | |
| X | X | | | | X | X | E0000-EFFFF | |
| X | X | | | | | X | F0000-FFFFF | |

X = Jumper installed

Figure 2-11. 20-Bit Memory Mapping

**Memory Mapping with the 16-Bit Address Bus:** There are three configurations for the 7709 when operating with a 16-bit address bus: no bank selection, 64K bank selection, and 32K bank selection. Each of these configurations is discussed below.

*No Bank Selection:* W3 must be configured as shown in figure 2-12 if bank selection is not used. In this configuration, the 7709 supports eight contiguously mapped memory sockets (MEM 0 through MEM 7) each capable of supporting an 8Kx8-bit memory device.

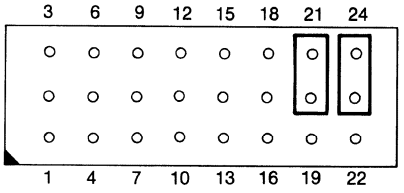



Figure 2-12. W3 Configured for No Bank Selection

It is important to note that the jumper in position 23-24 is used for MEMEX and may or may not be in the position shown in figure 2-12.

*64K Bank Selection:* W3 selects the bank address of the 64K bank on the 7709. If the data output to the bank select port matches the bank address, the memory will be enabled. For example, assume that the 7709 is to be configured for a 64K bank to be enabled when a hex 06 is output to the bank select port. Figure 2-13 shows W3 configured for a bank address of hex 06.

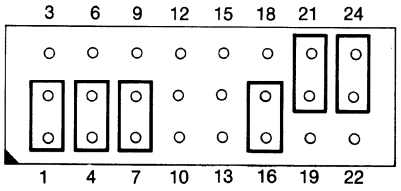



Figure 2-13. W3 Configured for a Bank Address of Hex 06

It is important to note that the jumper in position 23-24 is used for MEMEX and may or may not be in the position shown in figure 2-13.

Figure 2-14 provides the information necessary to configure W3 for a 64K bank address. If the 7709 is configured for bank address hex 3F, it will be enabled after reset and until a different bank address is output to the bank select port.

| W3 JUMPER POSITION | | | | | | | 64K BANK ADDRESS (HEX) |
|---|---|---|---|---|---|---|---|
| 1-2 (D5) | 4-5 (D4) | 7-8 (D3) | 10-11 (D2) | 13-14 (D1) | 16-17 (D0) | 20-21 — | |
| X | X | X | X | X | X | X | 00 |
| X | X | X | X | X | | X | 01 |
| X | X | X | X | | X | X | 02 |
| X | X | X | X | | | X | 03 |
| X | X | X | | X | X | X | 04 |
| X | X | X | | X | | X | 05 |
| X | X | X | | | X | X | 06 |
| X | X | X | | | | X | 07 |
| X | X | | X | X | X | X | 08 |
| X | X | | X | X | | X | 09 |
| X | X | | X | | X | X | 0A |
| X | X | | X | | | X | 0B |
| X | X | | | X | X | X | 0C |
| X | X | | | X | | X | 0D |
| X | X | | | | X | X | 0E |
| X | X | | | | | X | 0F |
| X | | X | X | X | X | X | 10 |
| X | | X | X | X | | X | 11 |
| X | | X | X | | X | X | 12 |
| X | | X | X | | | X | 13 |
| X | | X | | X | X | X | 14 |
| X | | X | | X | | X | 15 |
| X | | X | | | X | X | 16 |
| X | | X | | | | X | 17 |
| X | | | X | X | X | X | 18 |
| X | | | X | X | | X | 19 |
| X | | | X | | X | X | 1A |
| X | | | X | | | X | 1B |
| X | | | | X | X | X | 1C |
| X | | | | X | | X | 1D |
| X | | | | | X | X | 1E |
| X | | | | | | X | 1F |

| W3 JUMPER POSITION | | | | | | | 64K BANK ADDRESS (HEX) |
|---|---|---|---|---|---|---|---|
| 1-2 (D5) | 4-5 (D4) | 7-8 (D3) | 10-11 (D2) | 13-14 (D1) | 16-17 (D0) | 20-21 — | |
| | X | X | X | X | X | X | 20 |
| | X | X | X | X | | X | 21 |
| | X | X | X | | X | X | 22 |
| | X | X | X | | | X | 23 |
| | X | X | | X | X | X | 24 |
| | X | X | | X | | X | 25 |
| | X | X | | | X | X | 26 |
| | X | X | | | | X | 27 |
| | X | | X | X | X | X | 28 |
| | X | | X | X | | X | 29 |
| | X | | X | | X | X | 2A |
| | X | | X | | | X | 2B |
| | X | | | X | X | X | 2C |
| | X | | | X | | X | 2D |
| | X | | | | X | X | 2E |
| | X | | | | | X | 2F |
| | | X | X | X | X | X | 30 |
| | | X | X | X | | X | 31 |
| | | X | X | | X | X | 32 |
| | | X | X | | | X | 33 |
| | | X | | X | X | X | 34 |
| | | X | | X | | X | 35 |
| | | X | | | X | X | 36 |
| | | X | | | | X | 37 |
| | | | X | X | X | X | 38 |
| | | | X | X | | X | 39 |
| | | | X | | X | X | 3A |
| | | | X | | | X | 3B |
| | | | | X | X | X | 3C |
| | | | | X | | X | 3D |
| | | | | | X | X | 3E |
| | | | | | | X | 3F |

X = Jumper installed

Figure 2-14. 64K Bank Address Jumper Configuration

*32K Bank Selection:* W3 selects the bank addresses and the address range of the two 32K banks on the 7709. If the data output to the bank select port matches the bank address, the memory will be enabled. For example, assume that the 7709 is to be configured for two 32K banks that will occupy the address range of hex 0000 to 7FFF. One bank is to be enabled when a hex 0A is output to the bank select port and the other with a hex 0B.

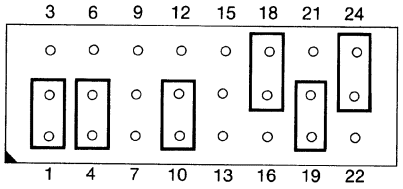



Figure 2-15. W3 Configured for Bank Address 0A and 0B Hex

It is important to note that the jumper in position 19-20 may be removed to redefine the address range as hex 8000 to FFFF. It is also important to note that the jumper in position 23-24 is used for MEMEX and may or may not be in the position shown.

Figure 2-16 provides the information necessary to configure W3 for 32K bank addresses. The lower bank address enables MEM 4 through 7 and the upper bank address enables MEM 0 through 3.

| W3 JUMPER POSITION | | | | | | | 32K BANK ADDRESS (HEX) | |
|---|---|---|---|---|---|---|---|---|
| 1-2 (D5) | 4-5 (D4) | 7-8 (D3) | 10-11 (D2) | 13-14 (D1) | 16-17 | 20-21 (1) | MEM 4-7 | MEM 0-3 |
| X | X | X | X | X | X | | 00 | 01 |
| X | X | X | X | | X | | 02 | 03 |
| X | X | X | | X | X | | 04 | 05 |
| X | X | X | | | X | | 06 | 07 |
| X | X | | X | X | X | | 08 | 09 |
| X | X | | X | | X | | 0A | 0B |
| X | X | | | X | X | | 0C | 0D |
| X | X | | | | X | | 0E | 0F |
| X | | X | X | X | X | | 10 | 11 |
| X | | X | X | | X | | 12 | 13 |
| X | | X | | X | X | | 14 | 15 |
| X | | X | | | X | | 16 | 17 |
| X | | | X | X | X | | 18 | 19 |
| X | | | X | | X | | 1A | 1B |
| X | | | | X | X | | 1C | 1D |
| X | | | | | X | | 1E | 1F |
| | X | X | X | X | X | | 20 | 21 |
| | X | X | X | | X | | 22 | 23 |
| | X | X | | X | X | | 24 | 25 |
| | X | X | | | X | | 26 | 27 |
| | X | | X | X | X | | 28 | 29 |
| | X | | X | | X | | 2A | 2B |
| | X | | | X | X | | 2C | 2D |
| | X | | | | X | | 2E | 2F |
| | | X | X | X | X | | 30 | 31 |
| | | X | X | | X | | 32 | 33 |
| | | X | | X | X | | 34 | 35 |
| | | X | | | X | | 36 | 37 |
| | | | X | X | X | | 38 | 39 |
| | | | X | | X | | 3A | 3B |
| | | | | X | X | | 3C | 3D |
| | | | | | X | | 3E | 3F |

X = Jumper installed
(1) Install for 32K bank address range hex 0000-7FFF; Remove for 32K bank address range hex 8000-8FFF.

Figure 2-16. 32K Bank Address Jumper Configuration

**MEMEX (W3):** MEMEX is an STD BUS signal that can be used to expand the amount of memory addressable by the CPU or for bootstrapping. Using W3, the 7709 can be configured to respond to MEMEX high, MEMEX low, or not to respond to MEMEX at all (disabled). Figure 2-17 shows W3 configured for MEMEX disabled. This is the as-shipped configuration for the 7709.

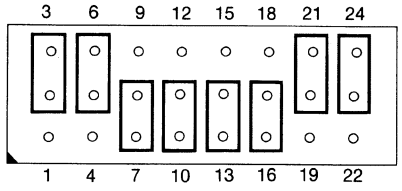



Figure 2-17. W3 Configured for MEMEX Disabled

It is important to note that only the right-most jumper position is used for MEMEX.

To enable MEMEX, refer to figure 2-4, page 2-3, for the correct jumper position. For example, assume that the memory on the 7709 is to be enabled only when MEMEX is in the high state. According to figure 2-4, this requires W3 with no jumper in positions 22-23 or 23-24.

**Memory Socket Configuration (W4, W7, W9, W10):** The 7709 has eight memory sockets (MEM 0 through MEM 7) that accept 8Kx8 memory devices. The memory sockets can be configured in groups of two for ROM, RAM without battery backup, or RAM with battery backup. W4 configures MEM 0-1; W7 configures MEM 2-3; W9 configures MEM 4-5, and W10 configures MEM 6-7. Refer to figure 2-4, page 2-3, for memory socket layout. Figure 2-18 shows all valid combinations of W4, W7, W9, and W10.

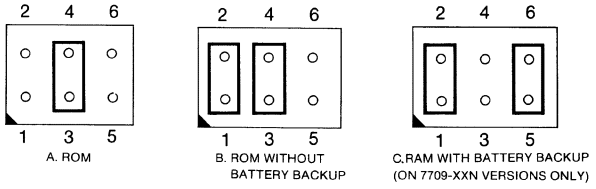



Figure 2-18. Memory Socket Configuration

Figure 2-4, page 2-3, provides the jumper information necessary to configure W4, W7, W9, and W10. For example, assume that W10 is to be configured for RAM with battery backup. According to figure 2-4, this would require jumpers placed only in positions 1-2 and 5-6. This is shown in figure 2-18C.

**Memory Socket Enable (W6):** The 7709 has eight memory sockets (MEM 0 through MEM 7) that can be independently enabled or disabled with W6. A memory socket must be disabled if it is mapped for an address range used somewhere other than the 7709. Figure 2-19 shows W6 configured to enable all eight memory sockets. This is the as-shipped configuration for the 7709.

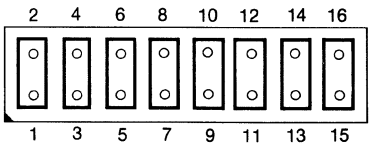



Figure 2-19. W6 Configured to Enable all Eight Memory Sockets

Figure 2-4, page 2-3, provides the jumper information necessary to configure W6. For example, assume that the 7709 is mapped for address range hex 00000 to 0FFFF. Also assume that the CPU card contains an 8K-byte ROM from hex 00000 to 01FFF. For this application, memory socket 0 on the 7709 must be disabled. According to figure 2-4, this would require that a jumper be removed from position 15-16 of W6.

## Battery Source Selection (W12):

The 7709-XXN versions are shipped with a nicad battery to provide data retention for battery-backed RAMs when power is removed. W12 provides the option of using the STD BUS VBATT (pin 5) signal in place of the nicad battery. Figure 2-19 shows W12 configured for the 7709-XXN nicad battery. This is the as-shipped configuration.

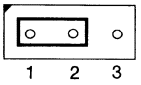



Figure 2-20. W12 Configured for the 7709-XXN Nicad Battery

Figure 2-4, page 2-3, provides the jumper information necessary to configure W12. For example, assume that the 7709 is to receive battery backup from the STD BUS VBATT power line. According to figure 2-4, this would require a jumper at position 2-3 of W12.

# Section 3
# OPERATION AND PROGRAMING

## INTRODUCTION

Section 3 explains the operation of the 7709. This explanation has been divided into four topics: 20-Bit Address Bus, 16-Bit Address Bus, Battery Backup, and Write Inhibit Switches.

## 20-BIT ADDRESS BUS

The 7709 operates in an STD BUS system with a 20-bit address bus (e.g., STD 8088). The 7709 decodes the lower 16 address lines (A0-A15) directly from the STD BUS. The upper four address lines (A16-A19) are demultiplexed from the lower four data lines (D0-D3) with the STD BUS MCSYNC* signal. This operation is totally transparent to the user.

Figure 3-1 shows each jumper group and how it affects a 7709 configured to operate with a 20-bit address bus.

| JUMPER GROUP | JUMPER POSITION | COMMENT | SEE PAGE |
|---|---|---|---|
| W1 | N/A | Any valid configuration | 2-4 |
| W2 | N/A | Any valid configuration | 2-5 |
| W3 | Variable | 20-bit address bus | 2-5, 3-2 |
| | Variable | MEMEX | 2-9 |
| W4 | Variable | MEM 0,1 socket configuration | 2-9 |
| W5 | | No bank selection | 2-5 |
| W6 | Variable | Memory socket enable | 2-9 |
| W7 | Variable | MEM 2,3 socket configuration | 2-9 |
| W8 | | 20-bit address bus | 2-5 |
| W9 | Variable | MEM 4,5 socket configuration | 2-9 |
| W10 | Variable | MEM 6,7 socket configuration | 2-9 |
| W11 | N/A | For Pro-Log use only | — |
| W12 | Variable | Battery backup source (on 7709-XXN versions only) | 2-9 |
| W13 | N/A | For Pro-Log use only | — |

N/A= Not Applicable. This jumper does not have to be considered for a 20-bit address bus operation.

Figure 3-1. Configuring the 7709 for a 20-Bit Address Bus

## Memory Mapping

The memory on the 7709 can be mapped anywhere within the address range provided by the 20-bit address bus. Figure 3-2 shows the address range of each memory socket for all sixteen jumper-selectable options.

| | MEMORY SOCKET | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| OPTION | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| AS SHIPPED | 00000-01FFF | 02000-03FFF | 04000-05FFF | 06000-07FFF | 08000-09FFF | 0A000-0BFFF | 0C000-0DFFF | 0E000-0FFFF |
| 1 | 10000-11FFF | 12000-13FFF | 14000-15FFF | 16000-17FFF | 18000-19FFF | 1A000-1BFFF | 1C000-1DFFF | 1E000-1FFFF |
| 2 | 20000-21FFF | 22000-23FFF | 24000-25FFF | 26000-27FFF | 28000-29FFF | 2A000-2BFFF | 2C000-2DFFF | 2E000-2FFFF |
| 3 | 30000-31FFF | 32000-33FFF | 34000-35FFF | 36000-37FFF | 38000-39FFF | 3A000-3BFFF | 3C000-3DFFF | 3E000-3FFFF |
| 4 | 40000-41FFF | 42000-43FFF | 44000-45FFF | 46000-47FFF | 48000-49FFF | 4A000-4BFFF | 4C000-4DFFF | 4E000-4FFFF |
| 5 | 50000-51FFF | 52000-53FFF | 54000-55FFF | 56000-57FFF | 58000-59FFF | 5A000-5BFFF | 5C000-5DFFF | 5E000-5FFFF |
| 6 | 60000-61FFF | 62000-63FFF | 64000-65FFF | 66000-67FFF | 68000-69FFF | 6A000-6BFFF | 6C000-6DFFF | 6E000-6FFFF |
| 7 | 70000-71FFF | 72000-73FFF | 74000-75FFF | 76000-77FFF | 78000-79FFF | 7A000-7BFFF | 7C000-7DFFF | 7E000-7FFFF |
| 8 | 80000-81FFF | 82000-83FFF | 84000-85FFF | 86000-87FFF | 88000-89FFF | 8A000-8BFFF | 8C000-8DFFF | 8E000-8FFFF |
| 9 | 90000-91FFF | 92000-93FFF | 94000-95FFF | 96000-97FFF | 98000-99FFF | 9A000-9BFFF | 9C000-9DFFF | 9E000-9FFFF |
| 10 | A0000-A1FFF | A2000-A3FFF | A4000-A5FFF | A6000-A7FFF | A8000-A9FFF | AA000-ABFFF | AC000-ADFFF | AE000-AFFFF |
| 11 | B0000-B1FFF | B2000-B3FFF | B4000-B5FFF | B6000-B7FFF | B8000-B9FFF | BA000-BBFFF | BC000-BDFFF | BE000-BFFFF |
| 12 | C0000-C1FFF | C2000-C3FFF | C4000-C5FFF | C6000-C7FFF | C8000-C9FFF | CA000-CBFFF | CC000-CDFFF | CE000-CFFFF |
| 13 | D0000-D1FFF | D2000-D3FFF | D4000-D5FFF | D6000-D7FFF | D8000-D9FFF | DA000-DBFFF | DC000-DDFFF | DE000-DFFFF |
| 14 | E0000-E1FFF | E2000-E3FFF | E4000-E5FFF | E6000-E7FFF | E8000-E9FFF | EA000-EBFFF | EC000-EDFFF | EE000-EFFFF |
| 15 | F0000-F1FFF | F2000-F3FFF | F4000-F5FFF | F6000-F7FFF | F8000-F9FFF | FA000-FBFFF | FC000-FDFFF | FE000-FFFFF |

Figure 3-2. 20-Bit Menory Mapping Options

The 7709 memory can be configured to system requirements using the memory mapping jumper group (W3) and the memory socket enable jumper group (W5).

For example, assume that the 7709 is to provide RAM from hex F0000 to F7FFF in an STD BUS system that contains ROM from hex F8000 to FFFFF. This is shown in figure 3-3.

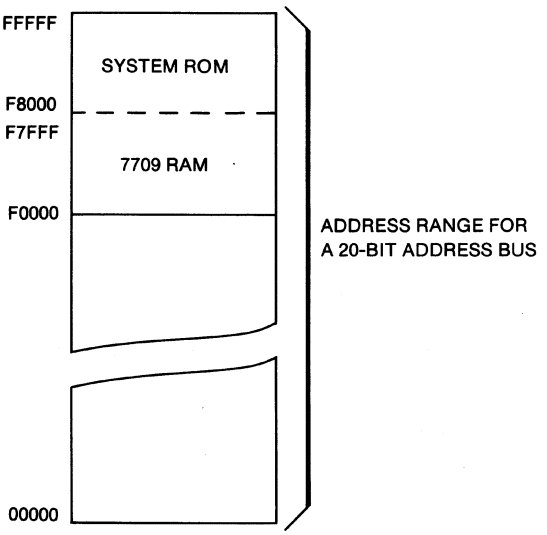



Figure 3-3. 20-Bit Memory Mapping Example

Option 15 of figure 3-2 shows memory sockets 0 through 3 mapped for hex F0000 to F7FFF. Since this meets the RAM requirements for this example, W3 would be configured for option 15. Option 15 also shows memory sockets 4 through 7 mapped from hex F8000 to FFFFF. These sockets must be jumper disabled with W5 to prevent contention with the system ROM mapped for the same address range.

## Memory Expansion With MEMEX

MEMEX is an STD BUS signal used to expand or enable memory. The 7709 can use MEMEX for memory expansion or bootstrapping if the CPU drives MEMEX through an output port. MEMEX can be used to select between two 7709 memory cards that are mapped for the same addressing space. This effectively doubles the CPU addressing space. The 7709 can also be made to respond to MEMEX in a state opposite that of a bootstrap ROM. In bootstrapping, the bootstrap ROM is enabled on system reset. After the bootstrapping operation is completed, the CPU complements the MEMEX signal to disable the ROM and enable the 7709 memory.

## Memory Expansion with Multiple 7709 Cards

From one to sixteen 7709 cards can be used to provide up to one megabyte of directly addressable memory. When using multiple 7709 cards, simply map each one for a different address range using W3.

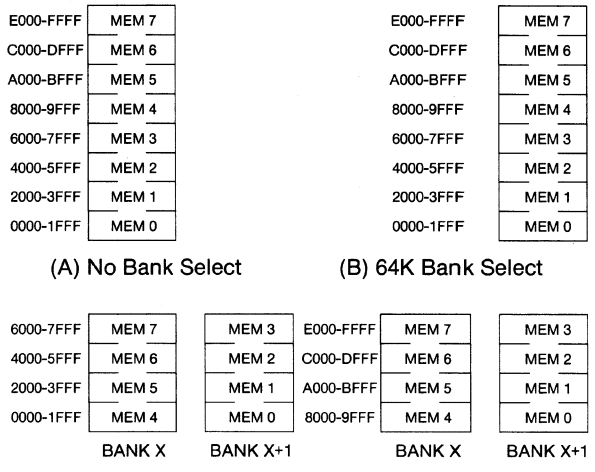
## 16-BIT ADDRESS BUS

The 7709 operates in an STD BUS system with a 16-bit address bus (e.g., STD 8085 and Z80). The 7709 decodes the 16 address lines (A0-A15) directly from the STD BUS. Figure 3-4 shows the four possible memory configurations of the 7709. Users who know which configuration to use may wish to skip the following discussion on bank selection.

## When to Use Bank Selection

An STD BUS system with a 16-bit address bus provides 64K bytes of directly addressable (primary) memory. Some applications may require more than 64K of combined RAM and ROM. This can be done by switching banks of memory into the 64K addressing space one at a time. This is shown in figure 3-5.

Each bank of memory has its own bank address. Each 7709 has a bank select port. If the data output to the bank select port matches the jumper-selectable bank address, the bank will be enabled into primary memory.




| CONFIGURATION | FIGURE | APPLICATION |
|---|---|---|
| No Bank Select | 3-4A | No more than 64K of memory in a system |
| 32K Bank Select | 3-4 C,D | More than 64K of memory in 32K or smaller contiguous blocks |
| 64K Bank Select | 3-4B | More than 64K of memory in 64K or smaller contiguous blocks |

Figure 3-4. 16-Bit Address Bus Options

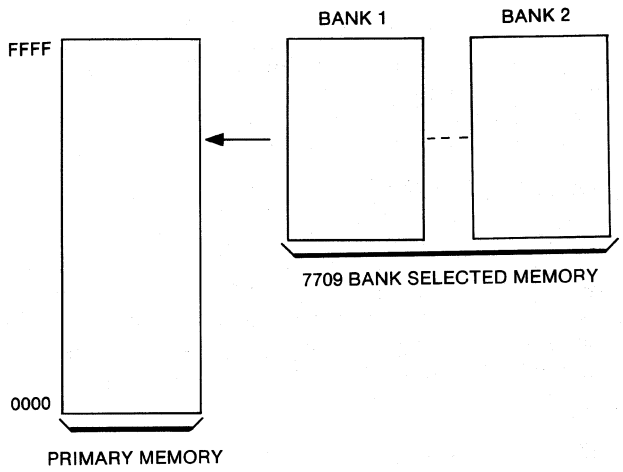


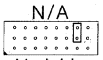

Figure 3-5. Bank Selection

The 7709 can be configured as one contiguous 64K bank (addressed from hex 0000 to FFFF) or two fully overlapped 32K banks (addressed from hex 0000 to 7FFF or 8000 to FFFF). The size of the bank depends upon system requirements.

## No Bank Selection

Figure 3-6 shows each jumper group and how it affects a 7709 configured to operate with a 16-bit address bus and no bank selection.

The memory on the 7709 can be mapped anywhere within the address range provided by the 16-bit address bus in 8K-byte blocks. Figure 3-4A shows the address range occupied by each empty socket on the 7709. The 7709 can be tailored to meet system needs by using only those memory sockets necessary. Other memory sockets can be jumper disabled with W5 if the memory is used elsewhere in the system.

| JUMPER GROUP | JUMPER POSITION | COMMENT | SEE PAGE |
|---|---|---|---|
| W1 | N/A | Any valid configuration | 2-4 |
| W2 | N/A | Any valid configuration | 2-5 |
| W3 |  | Memory mapping | 2-5 |
| | Variable | MEMEX | 2-9 |
| W4 | Variable | MEM 0,1 socket configuration | 2-9 |
| W5 |  | No bank selection | 2-3 |
| W6 | Variable | Memory socket enable | 2-9 |
| W7 | Variable | MEM 2,3 socket configuration | 2-9 |
| W8 | | 16-bit address bus | 2-5 |
| W9 | Variable | MEM 4,5 socket configuration | 2-9 |
| W10 | Variable | MEM 6,7 socket configuration | 2-9 |
| W11 | N/A | For Pro-Log use only | — |
| W12 | Variable | Battery backup source (on 7709-XXN versions only) | 2-9, 3-7 |
| W13 | N/A | For Pro-Log use only | — |

N/A= Not Applicable. This jumper does not have to be considered for a 16-bit address bus with no bank selection.

Figure 3-6. Configuring the 7709 for a 16-Bit Address Bus Without Bank Selection

## 64K Bank Selection

The memory on one 7709 can be mapped anywhere within the address range provided by the 16-bit address bus in 8K blocks. Figure 3-4B shows the address range occupied by each memory socket on the 7709. Using W3, multiple 7709s can be used by jumper configuring a different bank address for each. Each 7709 can be tailored to meet system requirements by using only the memory sockets necessary. Other memory sockets can be jumper disabled with W5 if the memory is used elsewhere in the system. Figure 3-7 shows each jumper group and how it affects a 7709 configured to operate with a 16-bit address bus and 64K bank selection.

| JUMPER GROUP | JUMPER POSITION | COMMENT | SEE PAGE |
|---|---|---|---|
| W1 | Variable | Bank select port mapping | 2-4 |
| W2 | Variable | IOEXP | 2-5 |
| W3 | Variable | Memory mapping | 2-5 |
| | Variable | MEMEX | 2-9 |
| W4 | Variable | MEM 0,1 socket configuration | 2-9 |
| W5 | | 64K Bank selection | 2-5 |
| W6 | Variable | Memory socket enable | 2-9 |
| W7 | Variable | MEM 2,3 socket configuration | 2-9 |
| W8 | | 16-bit address bus | 2-5 |
| W9 | Variable | MEM 4,5 socket configuration | 2-9 |
| W10 | Variable | MEM 6,7 socket configuration | 2-9 |
| W11 | N/A | For Pro-Log use only | — |
| W12 | Variable | Battery backup source (on 7709-XXN versions only) | 2-9, 3-7 |
| W13 | N/A | For Pro-Log use only | — |

N/A= Not Applicable. This jumper does not have to be considered for 16-bit address bus with 64K bank selection.

Figure 3-7. Configuring the 7709 for the 16-Bit Address Bus With 64K Bank Selection

For example, assume that an STD BUS system has 16K bytes of ROM mapped from hex 0000 to 3FFF. The system requires 96K bytes of RAM. This RAM can be supplied with two 7709 cards with 48K bytes on each. Figure 3-8 shows the memory map for this example.

The 7709 #1 is configured for bank address hex 00 using W3; 7709 #2 is configured for bank address hex 01 using W3. Memory sockets 0 and 1 on both 7709 cards can be jumper disabled with W5 to prevent contention with system ROM. Now, to select the RAM on either 7709 card simply output the correct bank address to the bank select port.

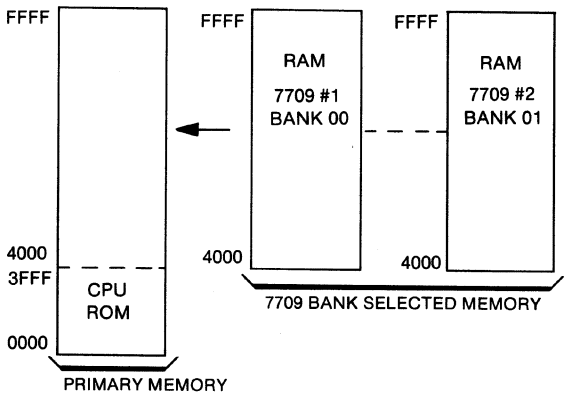



Figure 3-8. Bank Selecting 7709 Cards

## 32K Bank Selection

The memory on the 7709 can be mapped into two 32K banks that have the same memory address range and different bank addresses. Figure 3-4B and C show the address range occupied by each memory socket when the 7709 is used with 32K bank selection. Note that the upper four memory sockets (MEM 4 through 7) are enabled with the lower bank address (see figure 2-16). Each 32K bank can be tailored to meet system requirements by disabling the unused memory sockets for use elsewhere in the system.

Figure 3-9 shows each jumper group and how it affects the 7709 configured to operate with a 16-bit address bus and 32K bank selection.

| JUMPER GROUP | JUMPER POSITION | COMMENT | SEE PAGE |
|---|---|---|---|
| W1 | Variable | Bank select port mapping | 2-4 |
| W2 | Variable | IOEXP | 2-5 |
| W3 | Variable | Memory mapping | 2-9 |
| | Variable | MEMEX | 2-9 |
| W4 | Variable | MEM 0,1 socket configuration | 2-5 |
| W5 | | 32K Bank selection | 2-9 |
| W6 | Variable | Memory socket enable | 2-9 |
| W7 | Variable | MEM 2,3 socket configuration | 2-5 |
| W8 | | 16-bit address bus | 2-9 |
| W9 | Variable | MEM 4,5 socket configuration | 2-9 |
| W10 | Variable | MEM 6,7 socket configuration | 2-5 |
| W11 | N/A | For Pro-Log use only | — |
| W12 | Variable | Battery backup source (on 7709-XXN versions only) | 2-9, 3-7 |
| W13 | N/A | For Pro-Log use only | — |

N/A= Not Applicable. This jumper does not have to be considered for 16-bit address bus with 32K bank selection.

Figure 3-9. Configuring the 7709 for the 16-Bit Address Bus with 32K Bank Selection

For example, assume that an STD BUS system has 32K bytes of ROM mapped from hex 0000 to 7FFF. The system requires 96K bytes of RAM. This RAM can be supplied with two 7709 cards. One 7709 card can contain 64K bytes and the other 32K bytes. Figure 3-10 shows the memory map for this example.

The 7709 #1 is configured for bank addresses 00 and 01 hex using W3; the 7709 #2 is configured for bank addresses 02 and 03 using W3 (bank 03 is not needed for this example). Now, select the RAM on either 7709 card by simply outputting the correct bank address to the bank select port.

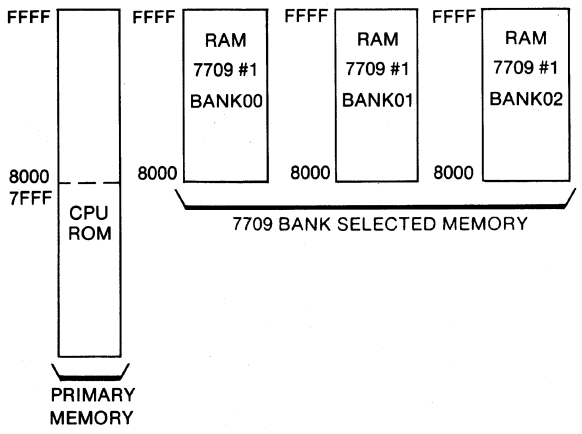



Figure 3-10. 32K Bank Selecting 7709 Cards

## Memory Expansion With MEMEX

The 7709 can use MEMEX for memory expansion or bootstrapping. MEMEX can be used to select between two 7709 memory cards that are mapped for the same addressing space. This effectively doubles the CPU addressing space. The 7709 can also be made to respond to MEMEX in a state opposite that of a bootstrap ROM. In bootstrapping, the bootstrap ROM is enabled on system reset. After the bootstrapping operation is completed, the CPU complements the MEMEX line to disable the ROM and enable the 7709 memory.

## Memory Expansion with Multiple 7709 Cards

A 16-bit address bus provides up to 64K bytes of directly addressable memory. One 7709 card can provide up to 64K bytes of memory to completely fill this addressing space. Two techniques can be used with the 7709 to obtain more than 64K of addressable memory.

MEMEX is an STD BUS signal that can be used if no more than 128K bytes of memory are required. MEMEX allows two 7709 cards to be mapped for the same address range with one enabled when MEMEX is high and the other with MEMEX low.

Software-programmable bank selection can be used when more than 64K bytes of memory are required. Each 7709 card is jumper configured for a different bank address. Only one of the 7709 cards will be enabled when an output instruction writes a bank address to the bank select port. For more information, refer to *When to Bank Select,* page 3-3.

The following example combines the use of MEMEX and software-programmable bank selection. Assume that the STD BUS system will power up with a 32K-byte boot ROM enabled with MEMEX low. The ROM is to be replaced by 64K bytes of RAM after the bootstrap operation is completed. The memory map for this application is shown in figure 3-11.

This application requires two 7709 cards each mapped for a different bank select port address. 7709 #1 must be configured to respond to MEMEX in a state opposite that of the ROM. The sequence of steps required to replace the ROM with 64K bytes of RAM is as follows:

1. The boot ROM outputs a hex 00 to the bank select port on the 7709 #2. This enables the RAM on the 7709 #2 into primary memory from hex 8000 to FFFF.
2. The boot ROM transfers the operating software into the enabled RAM. This eliminates the need for the boot ROM.
3. The operating software toggles the MEMEX line. This disables the boot ROM.
4. The operating software outputs hex 00 to the bank select port on the 7709 #1. This enables the RAM on the 7709 #1 into primary memory from hex 0000 to 7FFF. This application requires the two 7709s to be mapped for a different bank select port address. In general, this is not the case.

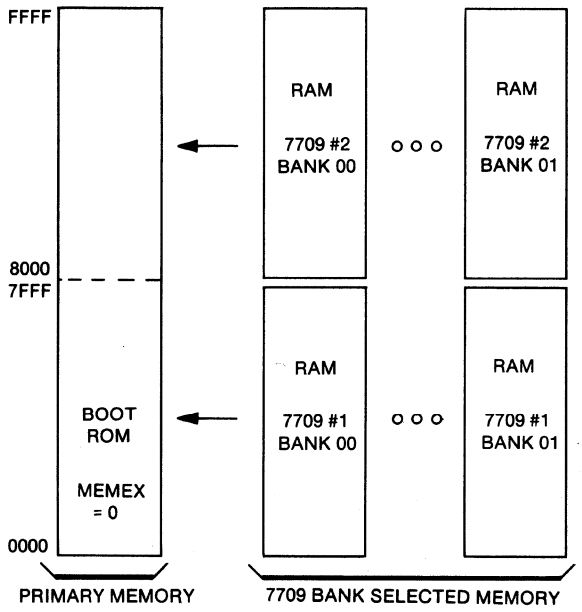



Figure 3-11. Using MEMEX and Bank Selection

## BATTERY BACKUP

The 7709-XXN has a nicad battery to provide data retention when power is removed.

### Data Retention Time

The data retention time is a measure of how long the 7709-XXN will retain data in a battery-backed RAM device. The following explains how to calculate and measure the data retention time.

**Calculating Data Retention Time:** The data retention time must be calculated to guarantee battery-backed data will not be lost in worst case conditions. The worst case (minimum) data retention times have been calculated for the 7709-XXN versions. These times are specified in Electrical Specifications, page 1-6.

The formula for calculating the data retention time is as follows:

$$T = \frac{2.916 \times 10^{-3}}{ISTBY}$$

T=Data retention time in days

ISTBY=RAM standby current(s) in microamps

For example, the 7709-16N has two RAM devices with a standby current of 50 microamps maximum and 20 microamps typical.

$$T(min) = \frac{2.916 \times 10^{-3}}{100+2} = 28.6 \text{ days}$$

$$T(typ) = \frac{2.916 \times 10^{-3}}{40+2} = 243 \text{ days}$$

The calculation for data retention is shown below:

**Measuring Data Retention Time:** The calculations above show that the typical value is more than eight times the worst case value. The standby current (ISTBY) can be measured and substituted into the above equation for a more accurate result. This works best if ISTBY can be measured in the environment in which the 7709 will be operating.

To measure the standby current from the battery:

1. Remove the 7709 from the STD BUS.
2. Remove the shorting receptacle from W12 pins 1-2.
3. Insert a microamp meter as shown in figure 3-12.

The measured value of ISTBY can then be used in the above formula for calculating the data retention time. This time is generally much longer than is shown by the worst-case calculation (assuming maximum ISTBY).

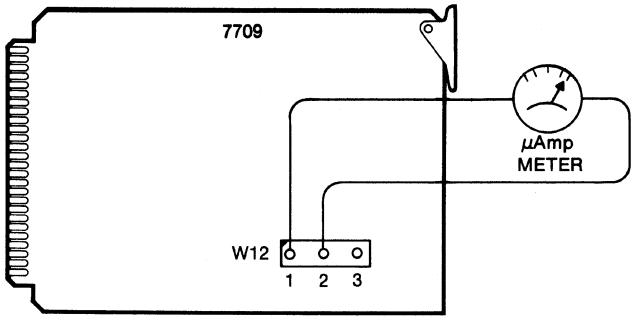



Figure 3-12. Measuring Battery Standby Current

## Powering Up and Down with Data Retention

The write inhibit switches must be used to guarantee data retention during power up and power down. The write inhibit switches in the "open" or "up" position prevent the CPU from writing data into memory during power transition periods.

NOTE: **Be sure the write inhibit switches are in the "OPEN" or "UP" position before applying power to or removing power from the 7709.**

Refer to the explanation below on Write Inhibit Switches for more information.

## Using VBATT for Battery Backup

The 7709 provides jumper group W12 to disconnect the nicad battery and connect the STD BUS VBATT (pin 5) power signal to provide battery backup. This is shown in figure 3-13. The voltage on VBATT must be between 3.3 and 4.5 volts. The battery used must be rechargeable unless R21 is removed from the 7709.

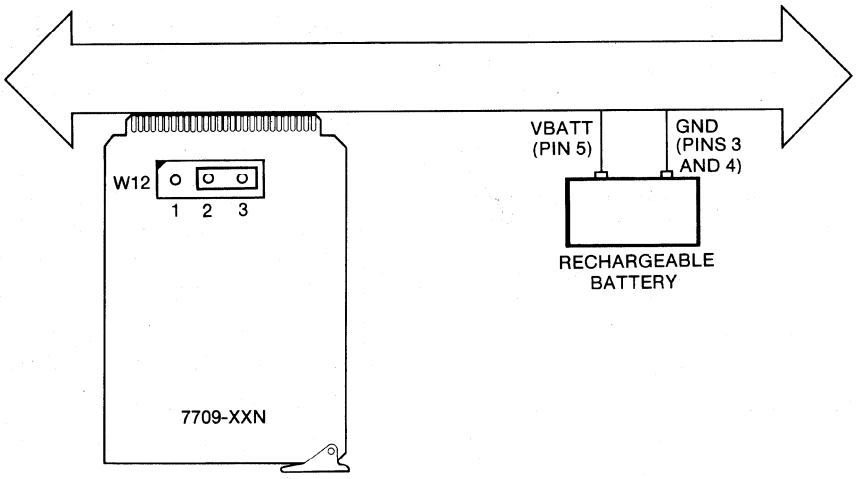



Figure 3-13. VBATT as a Source of 8attery Backup

## Battery Low Indication

The 7709 provides both visual and electrical indications when the battery voltage is too low to provide data retention. When the battery voltage is below 2.4V, the LED (DS1) illuminates and the normally high Battery Low* signal (J1 pin 2) goes low. When this happens, the 7709 should remain under power to recharge the battery. If the battery low indications are still active after 12 hours of charge, the battery must be replaced. It is important to note that the battery low indicators only function when power is applied to the 7709.

## WRITE INHIBIT SWITCHES

The 7709-XXN has four write inhibit switches. Each switch prevents the STD BUS write signal from reaching a socket pair when in the "open" or "up" position. Figure 3-14 shows the write inhibit switches and the memory socket pins they affect.

When a RAM device is write inhibited, it acts like a ROM device in that writing to it is not possible. This is useful for protecting debugged software during a software development phase.

These switches must also be used to write inhibit all battery-backed RAM when powering up or down the 7709 in an STD BUS system.

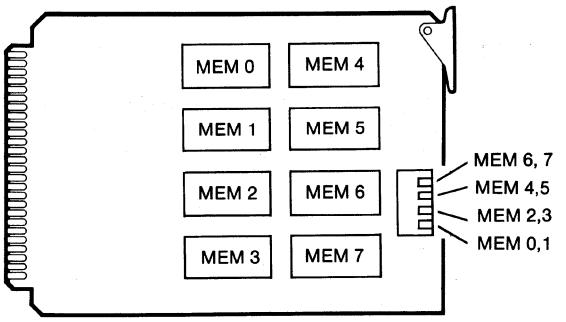



Figure 3-14. 7709-XXN Write Inhibit Switches

# Section 4
# OPERATING SOFTWARE

Section 4 is usually reserved for software for operation of an STD Series 7000 card. The 7709 card requires no operating software.

# Section 5
# MAINTENANCE

## REPLACING THE BATTERY

The following steps must be followed to replace the 7709-XXN battery.

1. Remove the 7709 from the STD BUS.
2. Remove the shorting receptacle from W12 pins 1-2.
3. Desolder and remove the battery and replace it with a new one. Batteries can be purchased from Pro-Log under Part number 902991.

## REFERENCE DRAWINGS

The schematics (figures 5-1 and 5-2) and assembly drawings (figures 5-3 and 5-4) in the following pages are included in this manual FOR REFERENCE USE ONLY. These drawings may differ in some respects from the card you receive from Pro-Log. If you require the specific revision documents of the schematic and assembly for the board shipped, please use the information request form in the back of this manual to order them.

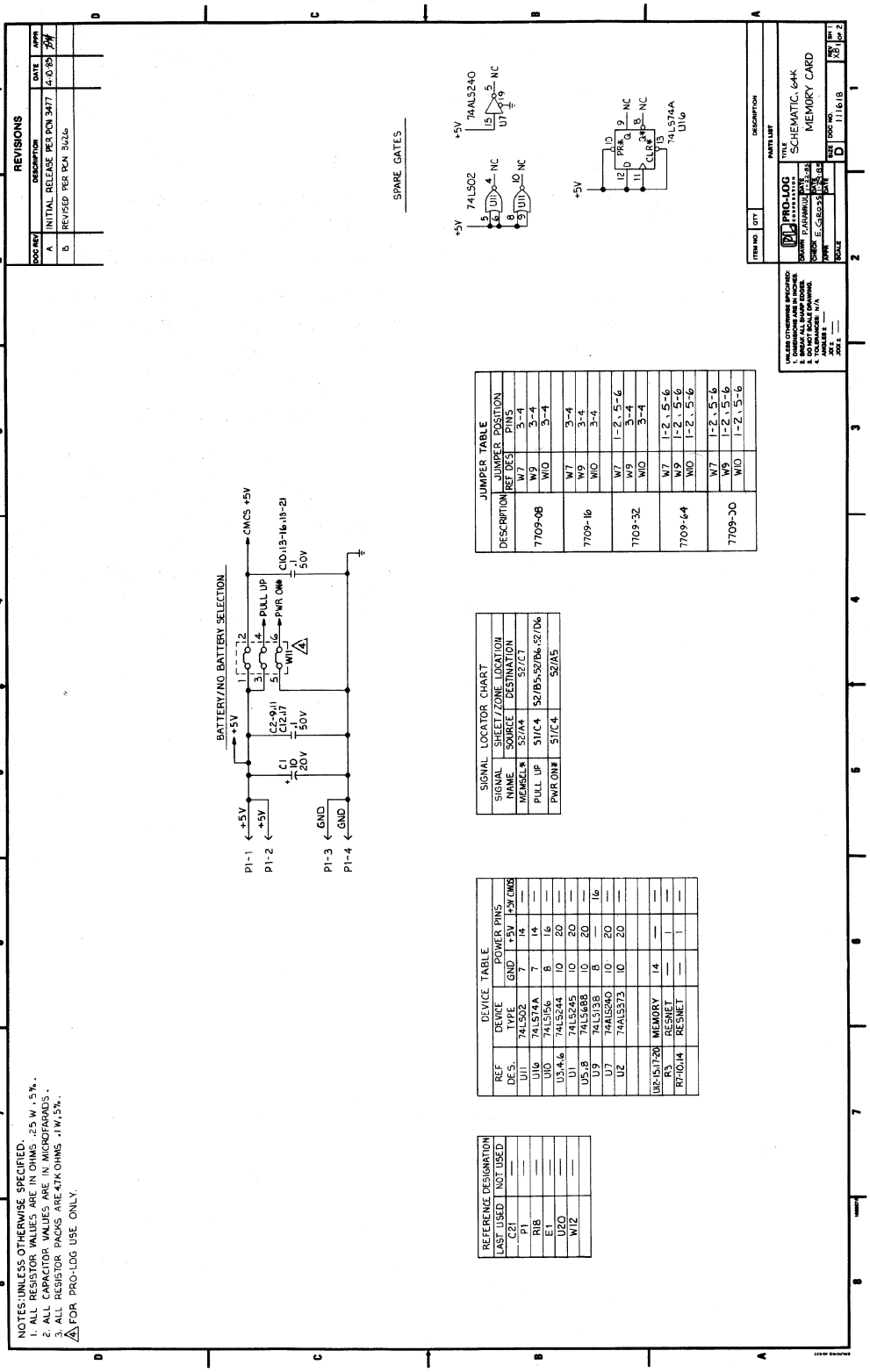



Figure 5-1. Schematic (page 1 of 2)
(7709-XXN with Battery Backup)

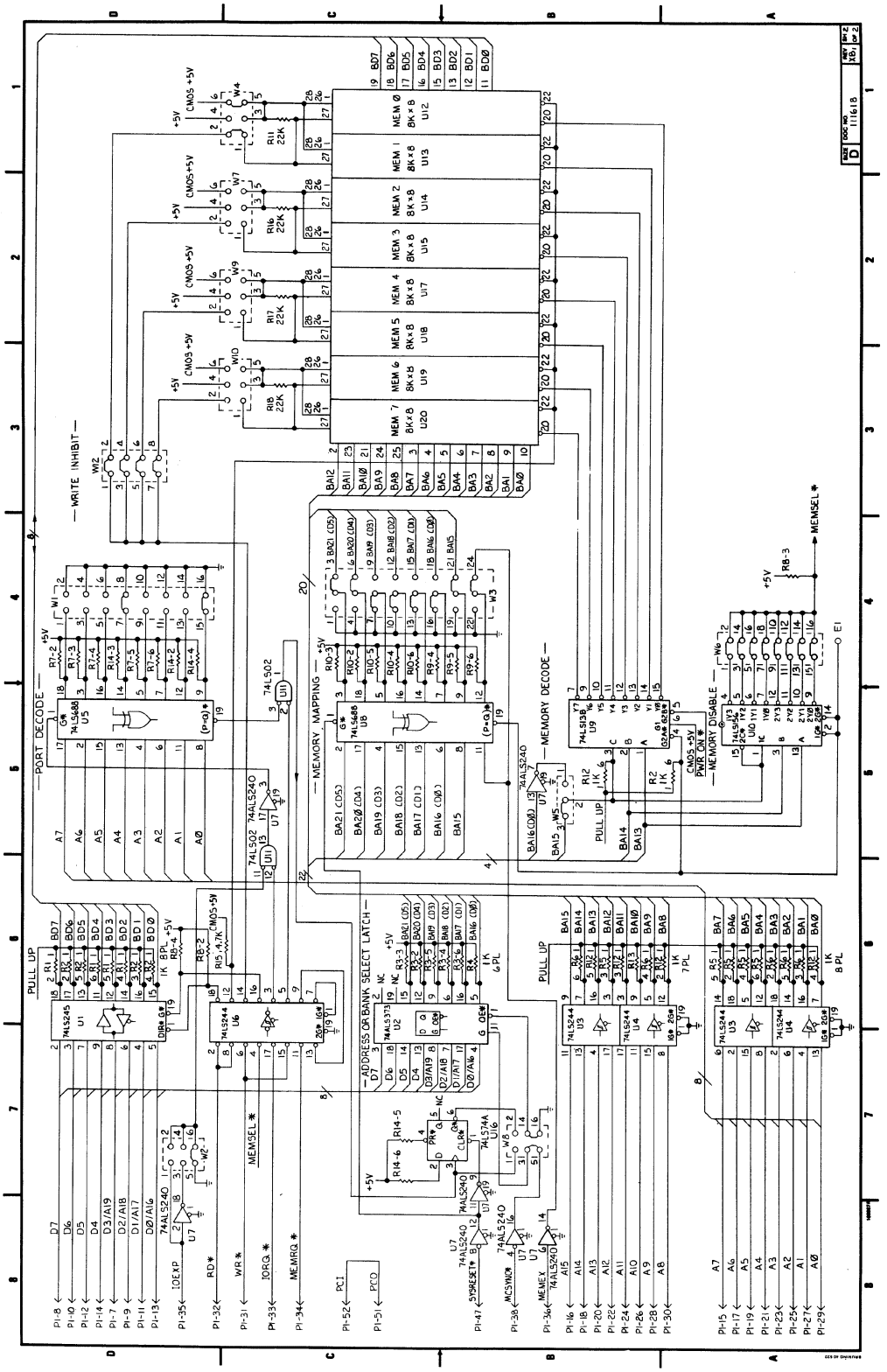


Figure 5-1. Schematic (page 2 of 2)
(7709-XXN with Battery Backup)

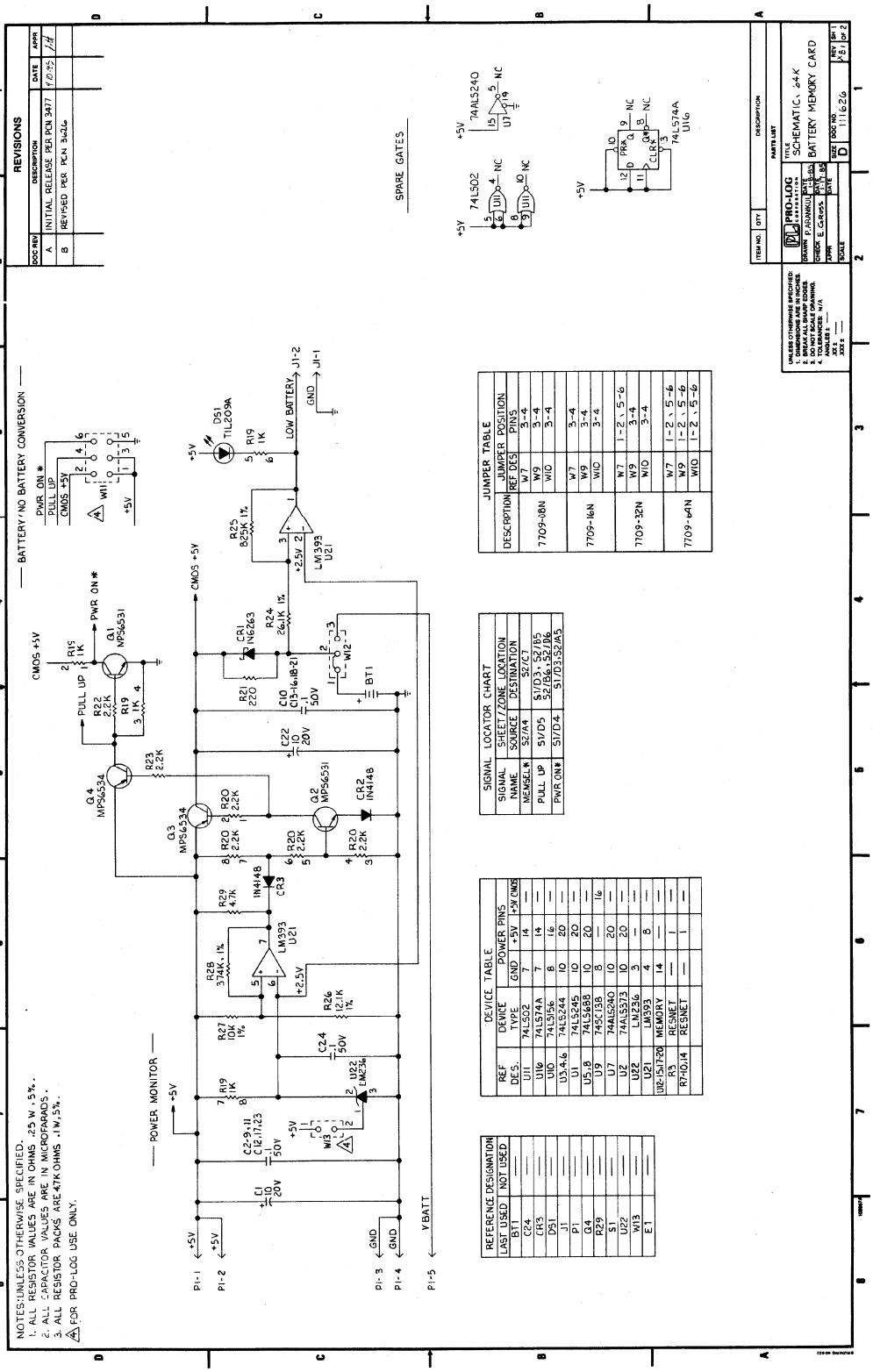


Figure 5-2. Schematic (page 1 of 2)
(7709-XX without Battery Backup)

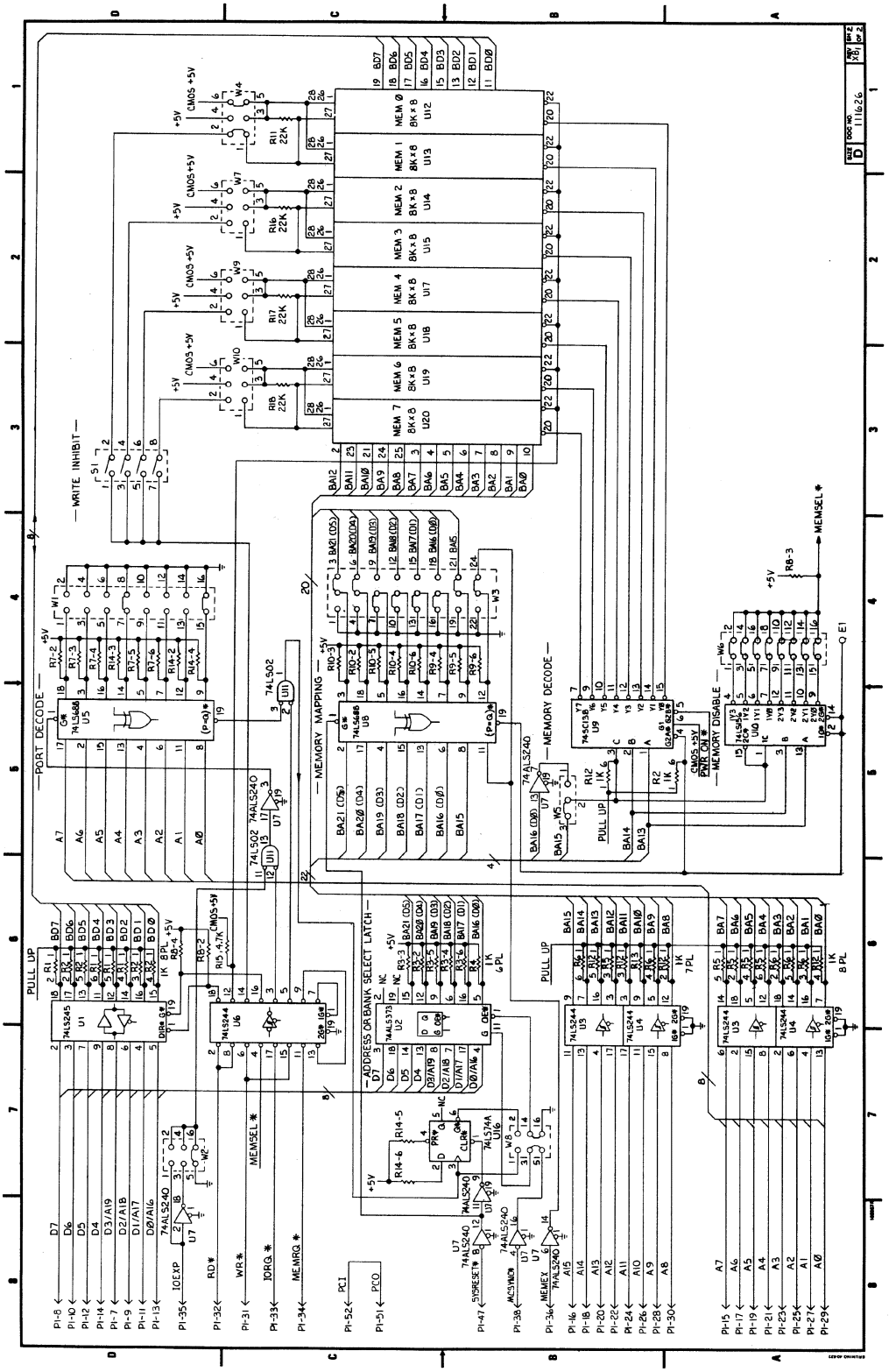


Figure 5-2. Schematic (page 2 of 2)
(7709-XX without Battery Backup)

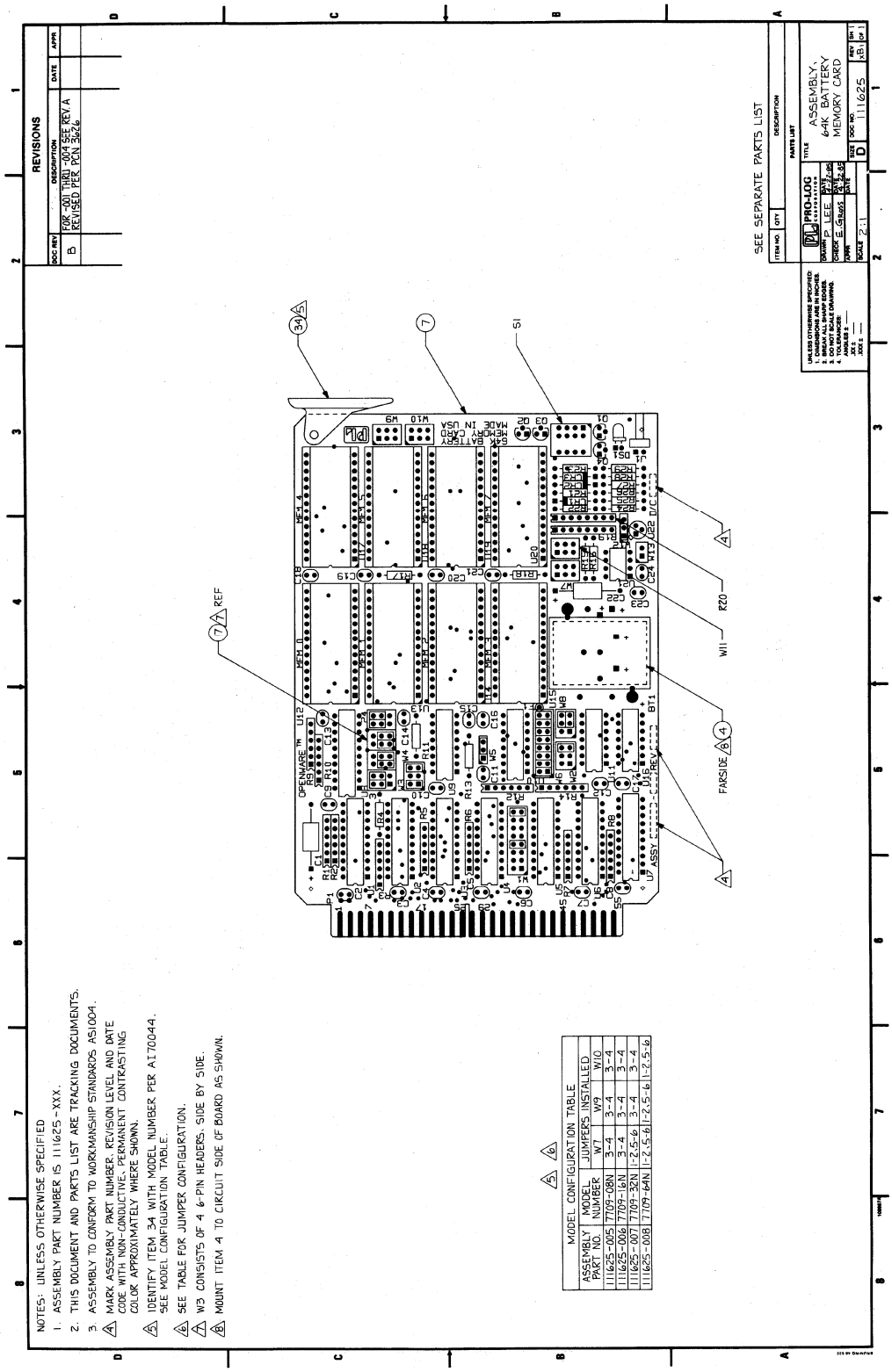
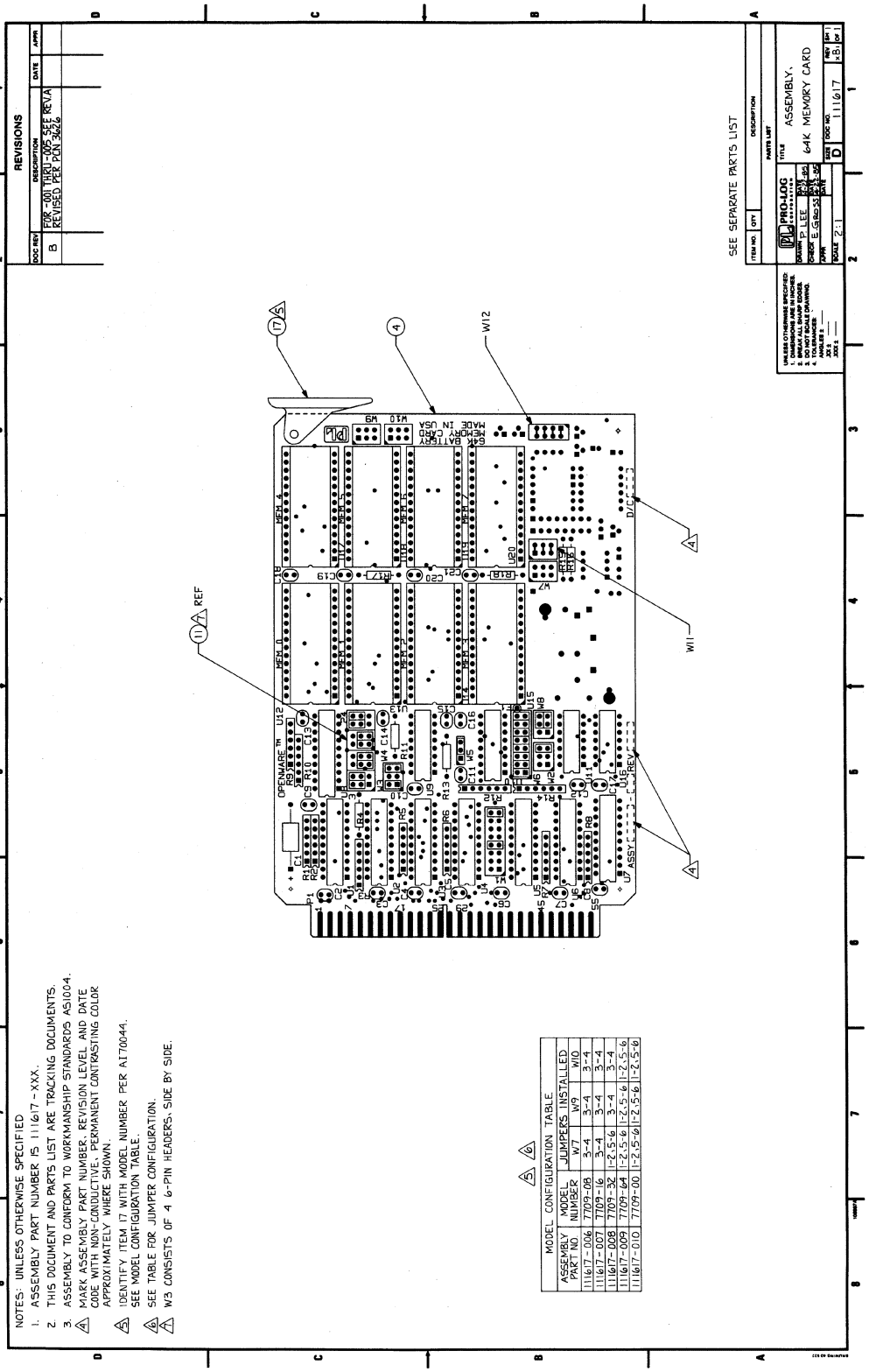



Figure 5-3. Assembly Drawing
(7709-XXN with Battery Backup)


REVISIONS
DOC REV
DESCRIPTION
DATE
APPR
B
PER -001 THRU -005 SEE REVA
REVISED PER PCN 3626
NOTES: UNLESS OTHERWISE SPECIFIED
1. ASSEMBLY PART NUMBER IS 111617-XXX.
2. THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS.
3. ASSEMBLY TO CONFORM TO WORKMANSHIP STANDARDS AS1004.
4. MARK ASSEMBLY PART NUMBER, REVISION LEVEL AND DATE CODE WITH NON-CONDUCTIVE, PERMANENT CONTRASTING COLOR APPROXIMATELY WHERE SHOWN.
5. IDENTIFY ITEM 17 WITH MODEL NUMBER PER AI70044.
6. SEE MODEL CONFIGURATION TABLE.
7. SEE TABLE FOR JUMPER CONFIGURATION.
8. W3 CONSISTS OF 4 6-PIN HEADERS, SIDE BY SIDE.
MODEL CONFIGURATION TABLE
ASSEMBLY PART NO.
MODEL NUMBER
JUMPERS INSTALLED
W7
W9
W10
111617-006
7709-08
3-4
3-4
3-4
111617-007
7709-16
3-4
3-4
3-4
111617-008
7709-32
1-2,5-6
3-4
3-4
111617-009
7709-64
1-2,5-6
1-2,5-6
2-4
111617-010
7709-00
1-2,5-6
1-2,5-6
1-2,5-6
SEE SEPARATE PARTS LIST
ITEM NO.
QTY
DESCRIPTION
PARTS LIST
PRO-LOG
DRAWN
CHECK
APPR
TITLE
ASSEMBLY, 64K MEMORY CARD
SIZE
D
DOC NO
111617
REV
B
SCALE 2:1
WEIGHT
SHEET 1 OF 1
UNLESS OTHERWISE SPECIFIED:
1. BREAK ALL SHARP EDGES.
2. DO NOT SCALE DRAWING.
ANGLES ± ___
XX ± ___
XXX ± ___
REF
W11
W12
W9
W10
W3
W7
W8
U12
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U48
U49
U50
U51
U52
U53
U54

## RETURN FOR REPAIR PROCEDURES

### Domestic Customers:

1. Call Customer Support at (800) 538-9570, ext. 3617. In California call (408) 646-3617 from 7 a.m. to 4 p.m. (Pacific Time).
2. Explain the problem and we may be able to solve it on the phone. If not, we will give you a Customer Return Order (CRO) number.

   Mark the CRO number on the shipping label, packing slip, and other paperwork accompanying the return. We cannot accept returns without a CRO.
3. Please be sure to enclose a packing slip with CRO number, serial number of the equipment, if applicable, and reason for return, with the name and telephone number of the person we should contact (preferably the user), if we have any further questions.
4. Pack the equipment in a solid cardboard box secured with packing material.

CAUTION

Loose MOS integrated circuits, or any product containing CMOS integrated circuits, must be protected from electrostatic discharge during handling. Use conductive foam pads or conductive plastic bags, and never place MOS or CMOS circuitry in contact with Styrofoam materials.

5. Ship prepaid and insured to:

   Pro-Log Corporation
   2411 Garden Road
   Monterey, California 93940

   Reference CRO #_____

### International Customers:

Equipment repair is handled by your local Pro-Log distributor. If you need to contact Pro-Log, the factory can be reached at any time by TWX at 910-360-7082.

## Limited Warranty

**Limited Warranty**: Seller warrants that the articles furnished hereunder are free from defects in material and workmanship and perform to applicable, published Pro-Log specifications for two years from date of shipment on PROM Programmers and STD BUS Series 7000 cards. This warranty is in lieu of any other warranty expressed or implied. In no event will Seller be liable for special or consequential damages as a result of any alleged breach of this warranty provision. The liability of Seller hereunder shall be limited to replacing or repairing, at its option, any defective units which are returned F.O.B. Seller's plant. Equipment or parts which have been subject to abuse, misuse, accident, alteration, neglect, unauthorized repair or installation are not covered by warranty. Seller shall have the right of final determination as to the existence and cause of defect. As to items repaired or replaced, the warranty shall continue in effect for the remainder of the warranty period, or for ninety (90) days following date of shipment by Seller of the repaired or replaced part whichever period is longer. No liability is assumed for expendable items such as lamps and fuses. No warranty is made with respect to custom equipment or products produced to Buyer's specifications except as specifically stated in writing by Seller and contained in the contract.

*Cut Here*

*FOLD*

*FOLD*

PRO-LOG® CORPORATION

**Yes, I'm interested in Pro-Log.**

**Please send me more information about your:**

- ☐ 7000 Series STD BUS Cards
- ☐ STD BUS Packaging Solutions
- ☐ STD BUS Subsystem
- ☐ STD BUS Systems
- ☐ Designer Software
- ☐ Design Courses and Seminars
- ☐ Programmer Product Line
- ☐ Other _____

- ☐ I am currently using Pro-Log equipment.
- ☐ Add my name to your mailing list.
- ☐ Please have a Sales Representative contact me.

Reader Comments: _____

Name _____ City _____

Company _____ State _____ Zip _____

Address _____ Telephone _____

PLACE
POSTAGE
HERE

PRO-LOG®
CORPORATION
2411 GARDEN ROAD
MONTEREY, CA 93940

Attn: Literature Department

# NOTES

# NOTES